



AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS
SINCE 1975

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INSTRUCTIONS

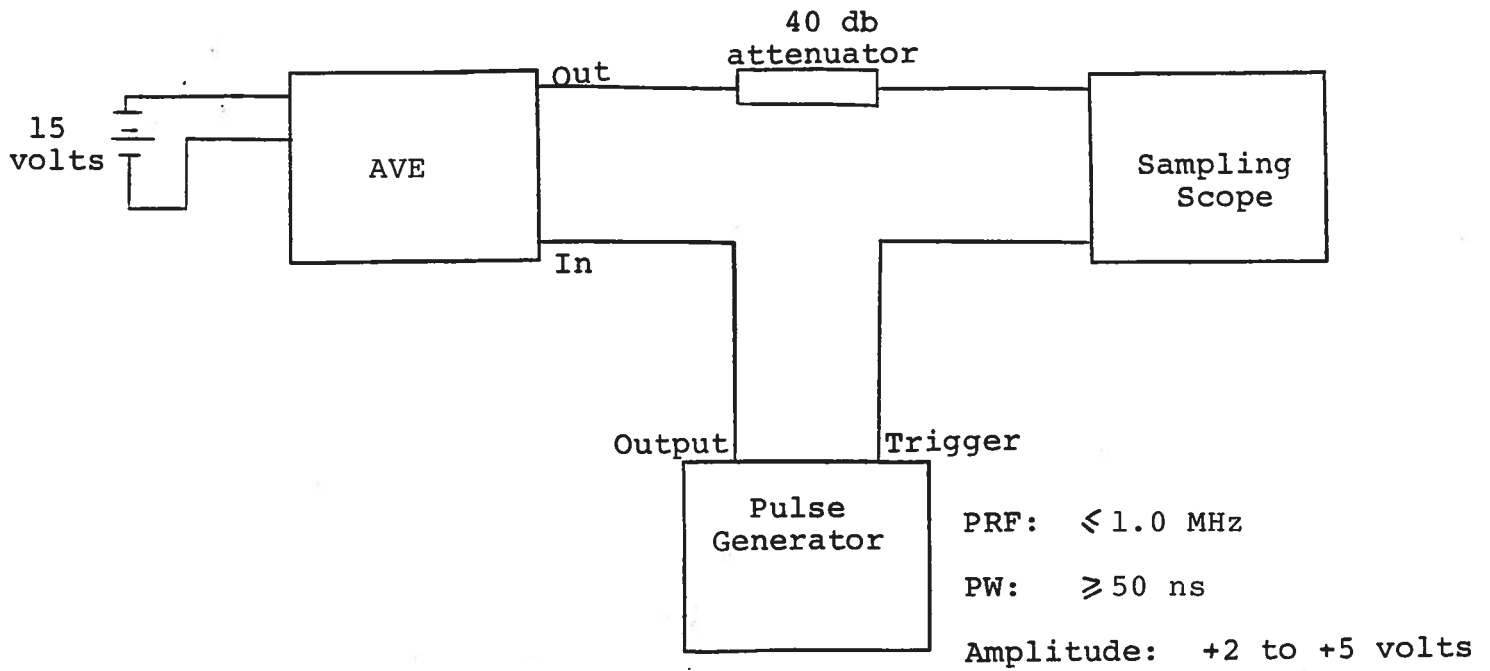
MODEL AVE MONOCYCLE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation or liability assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

MONOCYCLE GENERATOR TEST ARRANGEMENT



Notes:

- 1) The bandwidth capability of components and instruments used to display the monocycle generator output signal (attenuators, cables, connectors, etc.) should exceed 10 GHz.
- 2) The use of a 40 db attenuator will insure a peak input signal to the sampling scope of less than one volt.
- 3) In general, the pulse generator delay control should be set in the 100 ns range. Other settings should be as shown in the above diagram. The monocycle generator output is delayed with respect to the trigger input signal by about 75 ns (typically).
- 4) The monocycle generator can withstand an infinite VSWR on the output port.
- 5) The frequency of the output and the nature of the spurious following the monocycle may be varied by making minor adjustments to the two front panel trim pots located below the IN SMA.
- 6) For additional assistance:

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The circuit is a 1-bit full adder. It takes two 1-bit numbers and a carry-in as input and produces a 2-bit sum and a carry-out as output. The carry-in is connected to the carry-in input of the first full adder. The carry-out of the first full adder is connected to the carry-in of the second full adder. The carry-out of the second full adder is the carry-out of the circuit.

The circuit is a 2-bit full adder. It takes two 2-bit numbers and a carry-in as input and produces a 3-bit sum and a carry-out as output. The carry-in is connected to the carry-in input of the first full adder. The carry-out of the first full adder is connected to the carry-in of the second full adder. The carry-out of the second full adder is the carry-out of the circuit.

The circuit is a 4-bit full adder. It takes two 4-bit numbers and a carry-in as input and produces a 5-bit sum and a carry-out as output. The carry-in is connected to the carry-in input of the first full adder. The carry-out of the first full adder is connected to the carry-in of the second full adder. The carry-out of the second full adder is connected to the carry-in of the third full adder. The carry-out of the third full adder is the carry-out of the circuit.

The circuit is a 4-bit ripple carry adder. It takes two 4-bit numbers and a carry-in as input and produces a 5-bit sum and a carry-out as output. The carry-in is connected to the carry-in input of the first full adder. The carry-out of the first full adder is connected to the carry-in of the second full adder. The carry-out of the second full adder is connected to the carry-in of the third full adder. The carry-out of the third full adder is the carry-out of the circuit.

The circuit is a 4-bit ripple carry adder. It takes two 4-bit numbers and a carry-in as input and produces a 5-bit sum and a carry-out as output. The carry-in is connected to the carry-in input of the first full adder. The carry-out of the first full adder is connected to the carry-in of the second full adder. The carry-out of the second full adder is connected to the carry-in of the third full adder. The carry-out of the third full adder is the carry-out of the circuit.

For additional assistance

1st floor
1st floor