



AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS  
SINCE 1975

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## INSTRUCTIONS

MODEL AVRQ-5-B  
KILOVOLT PULSE GENERATOR  
WITH  $dV/dt$  RATES  
EXCEEDING 100 kV/us  
FOR COMMON MODE TRANSIENT IMMUNITY (CMTI) TESTS

SERIAL NUMBER: 14498



### WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been disassembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

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Manual Reference: /files/officefiles/instructword/avrq-5/AVRQ-5-B,sn14498.odt.  
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## INTRODUCTION

The AVRQ-5-B is designed to test the common mode transient immunity (CMTI) of optocouplers.

The standard AVRQ-5-B can generate -1.5 or +1.5 kV pulses. The unloaded switching time (10%-90%) is fixed at  $\leq 10$  ns. The transition time may be increased to at least 50 ns by adding high-voltage capacitors across the device under test (by soldering it to the DUT daughterboard). This corresponds to transition rates of  $< 24$  to  $> 120$  kV/us.

The -AHV option provides greater flexibility in the amplitude setting, permitting adjustment from 1.0 to 1.5 kV (+ or -) in  $\leq 1$ V steps.

The -XHV option provides a different amplitude range of 1.5 to 2.0 kV (+ or -) in  $\leq 1$ V steps, but the minimum switching time increases to 15 ns.

A daughterboard arrangement is used to accommodate different device packages and bias conditions. An arrangement of pin sockets on the main motherboard accepts these daughterboards. Eight daughterboards suitable for use with typical 5V DIP8 packages are included with the AVRQ-5-B. The CAD/CAM files for these sample boards are available for download at:

[https://www.avtechpulse.com/semiconductor/avrq-5/#support\\_files](https://www.avtechpulse.com/semiconductor/avrq-5/#support_files)

Users may design their own daughterboards to accommodate other package styles. (Earlier AVRQ-5-B units, prior to S/N 13700, used a different socketing and daughterboard arrangement. Current units have a different arrangement that offers lower parasitic inductance.)

The AVRQ-5-B mainframe provides the high-voltage common mode pulse (which is tied to GND1), and VCC2 / GND2 (the non-floating output-side power supply). The user is responsible for configuring the daughterboards to implement the correct input side power (VCC1), biasing, filtering, loading, socketing, and glitch measurement. The included sample boards implement these requirements for common DIP8 devices, using configurable jumpers/resistors/capacitors. A probe point is provided on the motherboard for observation of the device logic output with a user-provided probe and oscilloscope. An optional probe point is also provided on the sample daughterboards.

The ground-referenced output-side power (VCC2) is generated by the mainframe, and is adjustable (+3V to +43V, 150 mA maximum). The floating input-side power is not provided by the mainframe. Instead, an A23-type 12V battery should be installed on the DUT daughterboard to provide a floating power source, along with a basic regulator circuit to provide the necessary regulated +5V power (VCC1). A isolated battery arrangement is used to ensure that the VCC1 power supply is not the source of any glitches observed in the operation of the DUT.

The high-voltage pulse and the logic output of the DUT must be measured by the user, using suitable high-impedance oscilloscope probes. Coaxial cabling should not be used, because it will introduce too much parasitic capacitance.

The AVRQ-5-B features front panel keyboard and adjust knob control of the output pulse parameters along with a four line by 40-character backlit LCD display of the rise time, pulse width, pulse delay, and pulse repetition frequency. The instrument includes memory to store up to four complete instrument setups. The operator may use the front panel or the computer interface to store a complete “snapshot” of all key instrument settings, and recall this setup at a later time.

This instrument is intended for use in research, development, test and calibration laboratories by qualified personnel.

## HIGH-VOLTAGE PRECAUTIONS

 **CAUTION:** This instrument provides output voltages as high as 1500 or 2000 Volts under normal operating conditions, so extreme caution must be employed when using this instrument. The instrument should only be used by individuals who are thoroughly skilled in high voltage laboratory techniques. The following precautions should always be observed:

1. Keep exposed high-voltage wiring to an absolute minimum.
2. Wherever possible, use shielded connectors and cabling.
3. Connect and disconnect loads and cables only when the instrument is turned off.
4. Keep in mind that all cables, connectors, oscilloscope probes, and loads must have an appropriate voltage rating.

Do not attempt any repairs on the instrument, beyond the fuse replacement procedures described in this manual. Contact Avtech technical support (see page 2 for contact information) if the instrument requires servicing.



## SPECIFICATIONS

Model:	AVRQ-5-B <sup>1</sup>
High-Voltage Pulse Amplitude: (HV pulse / GND1)	Standard: -1.5 or +1.5 kV with -AHV <sup>5</sup> option: -1 kV to -1.5 kV, +1 kV to +1.5 kV, in $\leq 1V$ steps with -XHV <sup>6</sup> option: -1.5 kV to -2 kV, -1.5 kV to -2 kV, in $\leq 1V$ steps
Load resistance:	> 10 Megohms (this is not a 50 Ohm system.)
Load capacitance ( $C_{LOAD}$ ):	Standard: 0 to ~300 pF. -XHV units: 0 to ~1000 pF. Must be adjusted to obtain the desired transition time.
Load connection style:	A pattern of pin sockets into which a daughterboard may be plugged is provided. Sample daughterboards with 8-pin DIP sockets are included. The user may also use their own custom-made daughterboards.
Leading edge rise time for maximum output voltage <sup>2,8</sup> (10% - 90%):	Standard: $\leq 10$ ns (for $C_{LOAD} = 0$ pF), up to 50 ns. -XHV units: $\leq 15$ ns (for $C_{LOAD} = 0$ pF), up to 50 ns. Adjusted by varying $C_{LOAD}$ .
Leading edge shape:	Approximately linear. See the typical waveform photos on the preceding and following pages.
Trailing edge fall time (90%-10%):	At least ten times greater than the leading edge rise time. Not adjustable.
Trailing edge shape:	Exponential decay, approximately. See the typical waveform photos on the preceding and following pages.
Pulse width (measured between the start of the leading edge and the start of the falling edge):	1 - 20 $\mu$ s, adjustable.
PRF:	Standard: 10 Hz maximum -HF option: 100 Hz maximum
VCC1 power supply (input side, floating, referenced to HV pulse / GND1):	Not provided by the mainframe. The input side of the daughterboards must be self-powered. The included sample boards use an A23-type battery with a low-dropout regulator.
VCC2 power supply <sup>7</sup> (output side, referenced to GND2 chassis ground):	+3V to +43V, adjustable 150 mA maximum
Logic output pull-up resistance:	User-installed, on daughterboard as appropriate
Output connector, HV PULSE:	BNC female, suitable for use with the Tektronix P5100 high-voltage probe and 013-0291-00 probe-tip-to-BNC adapter. Other probes may be suitable. Not intended to drive any length of coaxial cabling directly.
Output connector, logic output:	A two-pin header suitable for use with the Tektronix P6246 differential probe <sup>4</sup> . Other probes may be used by installing a matching two-pin socket as an extender.
Output enable timer:	The output will only remain active for 90 seconds after the last output parameter update. After that time, the output will be disabled. The output must be re-enabled from the front panel or by computer command for the next test sequence.
Propagation delay:	$\leq 200$ ns (Ext trig in to start of output pulse)
Jitter (Ext trig in to pulse out):	$\pm 200$ ps $\pm 0.03\%$ of sync delay
Trigger modes:	Internal trigger, external trigger (TTL level pulse, > 10 ns, 1 k $\Omega$ input impedance), front-panel "Single Pulse" pushbutton, or single pulse trigger via computer command.
Variable delay:	Sync to Out: 0 to $\pm 1.0$ seconds, for all trigger modes (including external trigger).
Sync output:	+3 Volts, 100 ns, will drive 50 Ohm loads
Gate input:	Synchronous, active high or low, switchable. Suppresses triggering when active.
Other connectors:	Trig, Sync, Gate: BNC
GPIO and RS-232 control:	Yes. (Visit <a href="http://www.avtechpulse.com/labview">http://www.avtechpulse.com/labview</a> for LabView drivers.)
Ethernet port, for remote control using VXI-11.3, ssh, telnet, & web:	Included. Recommended as a modern alternative to GPIO / RS-232. See <a href="http://www.avtechpulse.com/options/vxi">http://www.avtechpulse.com/options/vxi</a> for details.
Settings accuracy:	Not calibrated. Verify the output parameters with a calibrated oscilloscope.
Power requirements:	100 - 240 Volts, 50 - 60 Hz
Dimensions: (H x W x D)	145 x 430 x 475 mm (5.7" x 17" x 18.8")
Chassis material:	cast aluminum frame and handles, blue vinyl on aluminum cover plates
Temperature range:	+5°C to +40°C

- 1) -B suffix indicates IEEE-488.2 GPIO and RS-232 control of amplitude, pulse width, PRF and delay (See <http://www.avtechpulse.com/gpio/>).
- 2) The rise time is affected by the load capacitance. A high-voltage high-bandwidth oscilloscope probe such as the Tektronix P5100 should always be used to verify the actual output rise time, rather than relying on the programmed value.
- 3) To specify the extended VCC2 range, add the -SCHB option suffix to the model number.
- 4) A differential probe is suggested to reduce the possibility of interference from the high-voltage pulse. Note that the P6246 is only suitable for values of VCC2 up to +7V. A non-differential probe may be more suitable if VCC2 > 7V, or if parasitic inductances or capacitances in the test circuit cause differential voltage spikes exceeding  $\pm 7V$ . The P6246 can saturate under those conditions, which can generate apparent glitch-like transients that are not due to the DUT. Some experimentation may be required by the user in order to identify the best probing arrangement.
- 5) Add the suffix -AHV to the model number to specify the +/- 1 to 1.5 kV (in  $\leq 1V$  steps) operating range.
- 6) Add the suffix -XHV to the model number to specify the +/- 1.5 to 2 kV (in  $\leq 1V$  steps) operating range. This option increases the minimum switching time by 5 ns.
- 7) VCC2 is normally provided at the DUT socket. It can also be provided on a BNC connector for monitoring purposes by specifying the -V2 option. The BNC connector will be on the same panel as the DUT enclosure (rear panel for standard units, front panel for -FPD units.) The shield of this BNC connector is connected to GND2 / chassis ground.
- 8) Valid with a Tektronix P5100 high-voltage probe connected directly to the HV PULSE connector. Connecting anything else (e.g., additional coaxial cabling or external DUTs) may degrade the switching times significantly.



## REGULATORY NOTES

### FCC PART 18

This device complies with part 18 of the FCC rules for non-consumer industrial, scientific and medical (ISM) equipment.

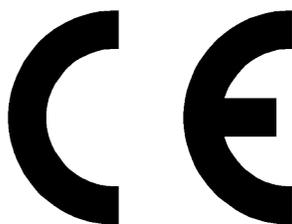
This instrument is enclosed in a rugged metal chassis and uses a filtered power entry module (where applicable). The main output signal is provided on a shielded connector that is intended to be used with shielded coaxial cabling and a shielded load. Under these conditions, the interference potential of this instrument is low.

If interference is observed, check that appropriate well-shielded cabling is used on the output connectors. Contact Avtech ([info@avtechpulse.com](mailto:info@avtechpulse.com)) for advice if you are unsure of the most appropriate cabling. Also, check that your load is adequately shielded. It may be necessary to enclose the load in a metal enclosure.

If any of the connectors on the instrument are unused, they should be covered with shielded metal “dust caps” to reduce the interference potential.

This instrument does not normally require regular maintenance to minimize interference potential. However, if loose hardware or connectors are noted, they should be tightened. Contact Avtech ([info@avtechpulse.com](mailto:info@avtechpulse.com)) if you require assistance.

### EC DECLARATION OF CONFORMITY



We                      Avtech Electrosystems Ltd.  
                             P.O. Box 5120, LCD Merivale  
                             Ottawa, Ontario  
                             Canada K2C 3H5

declare that this pulse generator meets the intent of Directive 2014/30/EU for Electromagnetic Compatibility. Compliance pertains to the following specifications as listed in the official Journal of the European Communities:

EN 50081-1 Emission

EN 50082-1 Immunity

and that this pulse generator meets the intent of the Low Voltage Directive 2014/35/EU. Compliance pertains to the following specifications as listed in the official Journal of the European Communities:

EN 61010-1:2010+A1:2019, Safety requirements for electrical equipment for measurement, control, and laboratory use

DIRECTIVE 2011/65/EU (RoHS)

We Avtech Electrosystems Ltd.  
P.O. Box 5120, LCD Merivale  
Ottawa, Ontario  
Canada K2C 3H5

declare that, to the best of our knowledge, all electrical and electronic equipment (EEE) sold by the company are in compliance with Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (also known as “RoHS Recast”). In addition, this declaration of conformity is issued under the sole responsibility of Avtech Electrosystems Ltd. Specifically, products manufactured do not contain the substances listed in the table below in concentrations greater than the listed maximum value.

<i>Material/Substance</i>	<i>Threshold level</i>
Lead (Pb)	< 1000 ppm (0.1% by mass)
Mercury (Hg)	< 1000 ppm (0.1% by mass)
Hexavalent Chromium (Cr6+)	< 1000 ppm (0.1% by mass)
Polybrominated Biphenyls (PBB)	< 1000 ppm (0.1% by mass)
Polybrominated Diphenyl ethers (PBDE)	< 1000 ppm (0.1% by mass)
Cadmium (Cd)	< 100 ppm (0.01% by mass)
Bis(2-ethylhexyl) phthalate (DEHP)	< 1000 ppm (0.1% by mass)
Butyl benzyl phthalate (BBP)	< 1000 ppm (0.1% by mass)
Dibutyl phthalate (DBP)	< 1000 ppm (0.1% by mass)
Diisobutyl phthalate (DIBP)	< 1000 ppm (0.1% by mass)

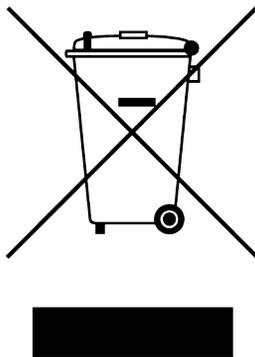
DIRECTIVE 2002/96/EC (WEEE)

European customers who have purchased this equipment directly from Avtech will have completed a “WEEE Responsibility Agreement” form, accepting responsibility for WEEE

compliance (as mandated in Directive 2002/96/EC of the European Union and local laws) on behalf of the customer, as provided for under Article 9 of Directive 2002/96/EC.

Customers who have purchased Avtech equipment through local representatives should consult with the representative to determine who has responsibility for WEEE compliance. Normally, such responsibilities will lie with the representative, unless other arrangements (under Article 9) have been made.

Requirements for WEEE compliance may include registration of products with local governments, reporting of recycling activities to local governments, and financing of recycling activities.



## FIRMWARE LICENSING

This instrument uses open-source software internally, and is built on a Fedora Linux operating system.

Some of this software requires that the source code be made available to the user as a condition of its licensing. The source code for programs used by Fedora is freely available at <https://src.fedoraproject.org/>.

The source code for modifications implemented by Avtech, and for Avtech-specific programs, is available at <https://www.avtechpulse.com/cgit/Instrument.git/>.



## INSTALLATION

### VISUAL CHECK

After unpacking the instrument, examine to ensure that it has not been damaged in shipment. Visually inspect all connectors, knobs, liquid crystal displays (LCDs), and the handles. Confirm that a power cord, a GPIB cable, and two instrumentation manuals (this manual and the “Programming Manual for -B Instruments”) are with the instrument. If the instrument has been damaged, file a claim immediately with the company that transported the instrument.

The following additional items should be with the instrument:

1. Eight assembled PCB 267D daughterboards
2. Eight A23-type 12V batteries

Additional items may be included, depending on the options ordered.

### POWER RATINGS

This instrument is intended to operate from 100 - 240 V, 50 - 60 Hz.

The maximum power consumption is 57 Watts. Please see the “FUSES” section for information about the appropriate AC and DC fuses.

This instrument is an “Installation Category II” instrument, intended for operation from a normal single-phase supply.

### CONNECTION TO THE POWER SUPPLY

An IEC-320 three-pronged recessed male socket is provided on the back panel for AC power connection to the instrument. One end of the detachable power cord that is supplied with the instrument plugs into this socket. The other end of the detachable power cord plugs into the local mains supply. Use only the cable supplied with the instrument. The mains supply must be earthed, and the cord used to connect the instrument to the mains supply must provide an earth connection. (The supplied cord does this.)

 Warning: Failure to use a grounded outlet may result in injury or death due to electric shock. This product uses a power cord with a ground connection. It must be connected to a properly grounded outlet. The instrument chassis is connected to the ground wire in the power cord.

The table below describes the power cord that is normally supplied with this instrument, depending on the destination region:

Destination Region	Description	Option	Manufacturer	Part Number
United Kingdom, Hong Kong, Singapore, Malaysia	BS 1363, 230V, 50 Hz	-AC00	Qualtek	370001-E01
Australia, New Zealand	AS 3112:2000, 230-240V, 50 Hz	-AC01	Qualtek	374003-A01
Continental Europe, Korea, Indonesia, Russia	European CEE 7/7 "Schuko" 230V, 50 Hz	-AC02	Qualtek	364002-D01
North America, Taiwan	NEMA 5-15, 120V, 60 Hz	-AC03	Qualtek	312007-01
Switzerland	SEV 1011, 230V, 50 Hz	-AC06	Qualtek	378001-E01
South Africa, India	SABS 164-1, 220-250V, 50 Hz	-AC17	Volex	2131H 10 C3
Japan	JIS 8303, 100V, 50-60 Hz	-AC18	Qualtek	397002-01
Israel	SI 32, 220V, 50 Hz	-AC19	Qualtek	398001-01
China	GB 1002-1 / 2099-1, 220V, 50 Hz	-AC22	Qualtek	399012-01

## PROTECTION FROM ELECTRIC SHOCK

 Operators of this instrument must be protected from electric shock at all times. The owner must ensure that operators are prevented access and/or are insulated from every connection point. In some cases, connections must be exposed to potential human contact. Operators must be trained to protect themselves from the risk of electric shock. This instrument is intended for use by qualified personnel who recognize shock hazards and are familiar with safety precautions required to avoid possibly injury. In particular, operators should:

1. Keep exposed high-voltage wiring to an absolute minimum.
2. Wherever possible, use shielded connectors and cabling.
3. Connect and disconnect loads and cables only when the instrument is turned off.
4. Keep in mind that all cables, connectors, oscilloscope probes, and loads must have an appropriate voltage rating.
5. Do not attempt any repairs on the instrument, beyond the fuse replacement procedures described in this manual. Contact Avtech technical support (see page 2 for contact information) if the instrument requires servicing. Service is to be performed solely by qualified service personnel.

## ENVIRONMENTAL CONDITIONS

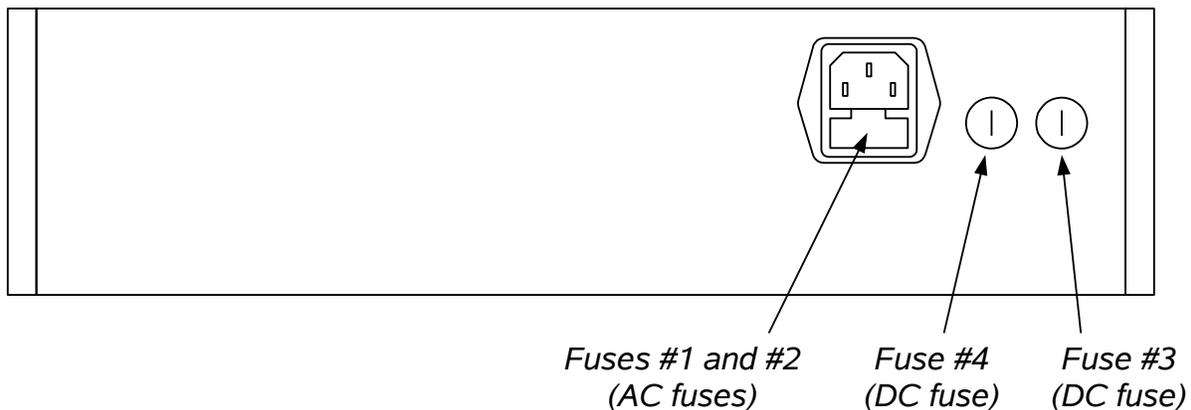
This instrument is intended for use under the following conditions:

1. indoor use;
2. altitude up to 2 000 m;
3. temperature 5 °C to 40 °C;
4. maximum relative humidity 80 % for temperatures up to 31 °C decreasing linearly to 50 % relative humidity at 40 °C;
5. Mains supply voltage fluctuations up to  $\pm 10$  % of the nominal voltage;
6. no pollution or only dry, non-conductive pollution.



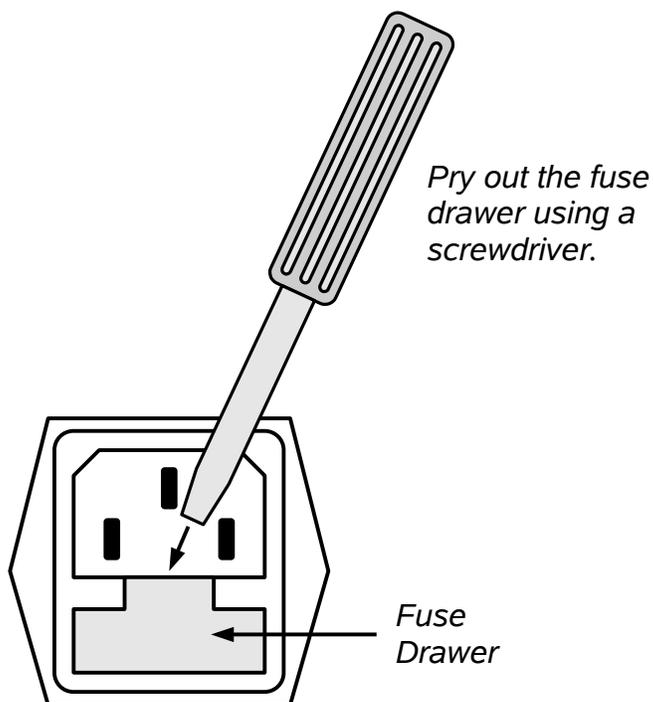
## FUSES

This instrument contains four fuses. All are accessible from the rear-panel. Two protect the AC prime power input, and two protect the internal DC power supplies. The locations of the fuses on the rear panel are shown in the figure below:



### AC FUSE REPLACEMENT

To physically access the AC fuses, the power cord must be detached from the rear panel of the instrument. The fuse drawer may then be extracted using a small flat-head screwdriver, as shown below:



## DC FUSE REPLACEMENT

The DC fuses may be replaced by inserting the tip of a flat-head screwdriver into the fuse holder slot, and rotating the slot counter-clockwise. The fuse and its carrier will then pop out.

## FUSE RATINGS

The following table lists the required fuses:

Fuses	Nominal Mains Voltage	Rating	Case Size	Recommended Replacement Part	
				Littelfuse Part Number	Digi-Key Stock Number
#1, #2 (AC)	100-240V	0.5A, 250V, Time-Delay	5×20 mm	0218.500HXP	F2416-ND
#3 (DC)	N/A	1.0A, 250V, Time-Delay	5×20 mm	0218001.HXP	F2419-ND
#4 (DC)	N/A	0.5A, 250V, Time-Delay	5×20 mm	0218.500HXP	F2416-ND

The recommended fuse manufacturer is Littelfuse (<http://www.littelfuse.com>).

Replacement fuses may be easily obtained from Digi-Key (<http://www.digikey.com>) and other distributors.

## CHASSIS CONFIGURATIONS

The AVRQ-5-B is offered with two basic chassis configurations. The standard model is provided in a “3U” height (in rack units) enclosure, with the DUT area located on the rear panel.

The DUT area may optionally be moved to the front panel by specifying the -FPD option. This is more convenient for the user, but it increases the height of the instrument from 3U to 5U, and higher shipping costs may apply.

### STANDARD CONFIGURATION



Front



Rear

### -FPD CONFIGURATION



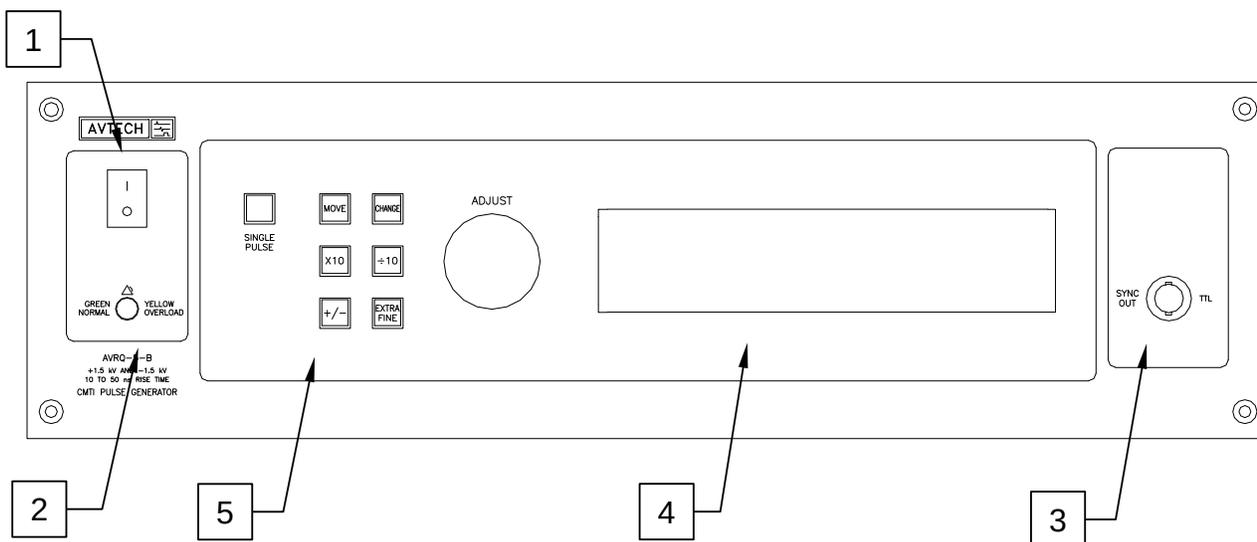
Front



Rear



## FRONT PANEL CONTROLS (UNITS WITHOUT -FPD OPTION)



1. POWER Switch. This is the main power switch. When turning the instrument on, there is normally a delay of 10 seconds before anything is shown on the main display, as the internal operating system boots up.

2. OVERLOAD Indicator. When the instrument is powered, this indicator is normally green, indicating normal operation. If this indicator is yellow, an internal automatic overload protection circuit has been tripped. If the unit is overloaded (by operating at an exceedingly high duty cycle or by operating into a very low impedance), the protective circuit will disable the output of the instrument and turn the indicator light yellow. The light will stay yellow (i.e. output disabled) for about 5 seconds after which the instrument will attempt to re-enable the output (i.e. light green) for about 1 second. If the overload condition persists, the output will be disabled again (i.e. light yellow) for another 5 seconds. If the overload condition has been removed, the instrument will resume normal operation.

This overload indicator may flash yellow briefly at start-up. This is not a cause for concern.

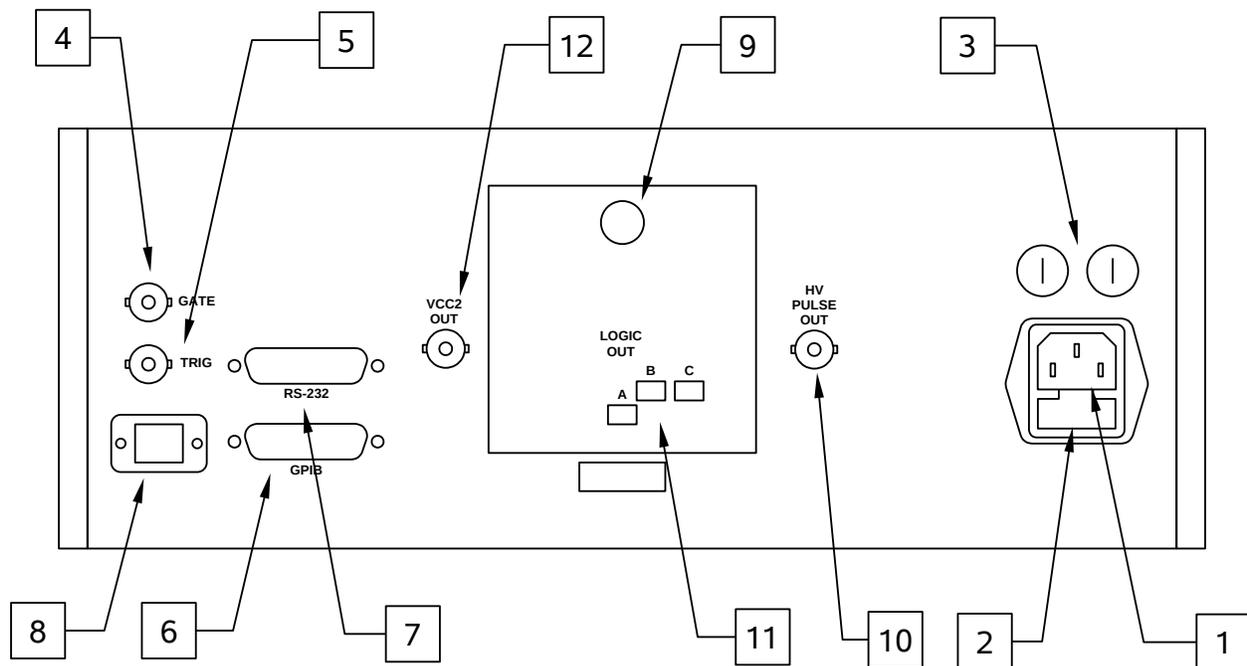
3. SYNC OUT. This connector supplies a SYNC output that can be used to trigger other equipment, particularly oscilloscopes. This signal leads (or lags) the main output by a duration set by the "DELAY" controls and has an approximate amplitude of +3 Volts to  $R_L > 1\text{ k}\Omega$  with a pulse width of approximately 100 ns.

4. LIQUID CRYSTAL DISPLAY (LCD). This LCD is used in conjunction with the keypad to change the instrument settings. Normally, the main menu is displayed, which lists the key adjustable parameters and their current values. The "Programming Manual for -B Instruments" describes the menus and submenus in detail.

5. KEYPAD.

Control Name	Function
MOVE	This moves the arrow pointer on the display.
CHANGE	This is used to enter the submenu, or to select the operating mode, pointed to by the arrow pointer.
×10	If one of the adjustable numeric parameters is displayed, this increases the setting by a factor of ten.
÷10	If one of the adjustable numeric parameters is displayed, this decreases the setting by a factor of ten.
+/-	If one of the adjustable numeric parameters is displayed, and this parameter can be both positive or negative, this changes the sign of the parameter.
EXTRA FINE	This changes the step size of the ADJUST knob. In the extra-fine mode, the step size is twenty times finer than in the normal mode. This button switches between the two step sizes.
ADJUST	This large knob adjusts the value of any displayed numeric adjustable values, such as frequency, pulse width, etc. The adjust step size is set by the "EXTRA FINE" button.  When the main menu is displayed, this knob can be used to move the arrow pointer.

REAR PANEL CONTROLS (UNITS WITHOUT -FPD OPTION)



*Note: some connectors may be in different positions than shown above, depending on the exact combination of options ordered.*

1. AC POWER INPUT. An IEC-320 C14 three-pronged recessed male socket is provided on the back panel for AC power connection to the instrument. One end of the detachable power cord that is supplied with the instrument plugs into this socket.
2. AC FUSE DRAWER. The two fuses that protect the AC input are located in this drawer. Please see the “FUSES” section of this manual for more information.
3. DC FUSES. These two fuses protect the internal DC power supplies. Please see the “FUSES” sections of this manual for more information.
4. GATE. This TTL-level (0 and +5V) logic input can be used to gate the triggering of the instrument. This input can be either active high or active low, depending on the front panel settings or programming commands. (The instrument triggers normally when this input is unconnected). When set to active high mode, this input is pulled-down to ground by a 1 k $\Omega$  resistor. When set to active low mode, this input is pulled-up to +5V by a 1 k $\Omega$  resistor.
5. TRIG. This TTL-level (0 and +5V) logic input can be used to trigger the instrument, if the instrument is set to triggering externally. The instrument triggers

on the rising edge of this input. The input impedance of this input is 1 k $\Omega$ . (Depending on the length of cable attached to this input, and the source driving it, it may be desirable to add a coaxial 50 Ohm terminator to this input to provide a proper transmission line termination. The Pasternack ([www.pasternack.com](http://www.pasternack.com)) PE6008-50 BNC feed-thru 50 Ohm terminator is suggested for this purpose.)

6. GPIB Connector. A standard GPIB cable can be attached to this connector to allow the instrument to be computer-controlled. See the “Programming Manual for -B Instruments” for more details on GPIB control.
7. RS-232 Connector. A standard serial cable with a 25-pin male connector can be attached to this connector to allow the instrument to be computer-controlled. A user name (“admin”) and a password (“default”, as shipped from the factory) are required when logging into a serial terminal session. The internal controller attempts to auto-sense the parity setting. It may be necessary to send a few return characters before attempting a login in order to provide enough data to allow this auto-sensing to work. (A standard Linux “agetty” process is used to implement serial control internally.) See the “Programming Manual for -B Instruments” for more details on RS-232 control.
8. Network Connector. This Ethernet connector allows the instrument to be remotely controlled using the VXI-11.3, ssh (secure shell), telnet, and http (web) protocols. See the “Programming Manual for -B Instruments” for more details.
9. DUT Door. This is the door that provides access to the DUT socket. To open it, pull on the chrome knob. When closed, the door is held latched in place magnetically.

The high voltage output is automatically disabled when the DUT door is opened. The door must be closed during tests.

10. HV PULSE OUT CONNECTOR. The BNC connector provides access to the high voltage (up to  $\pm 2$  kV) pulse that is applied to the DUT, for monitoring purposes. This signal must be observed on an oscilloscope to accurately measure the dV/dt rate of the high voltage pulse.

A Tektronix P5100 high-voltage probe with the 013-0291-00 probe-tip-to-BNC adapter, or a similar arrangement, should be used to connect to this output.

 CAUTION: Voltages as high as 2 kV may be present on the center conductor of this output connector. Avoid touching this conductor. Connect to this connector using a Tektronix P5100 high-voltage probe with the 013-0291-00 probe-tip-to-BNC adapter, or a similar arrangement, to ensure that the center conductor is not exposed.

 DO NOT CONNECT THIS OUTPUT DIRECTLY TO AN OSCILLOSCOPE. The oscilloscope will be damaged by the high voltages. Use a Tektronix P5100 high-voltage probe with the 013-0291-00 probe-tip-to-BNC adapter, or a similar

arrangement.

 DO NOT CONNECT COAXIAL CABLING TO THIS OUTPUT. The capacitance of the cabling will reduce the dV/dt rates noticeably.

11. LOGIC OUT Connectors. There are three possible positions where the logic probe can be connected, “A”, “B”, and “C”.

“A” is a two-pin header connector mounted on the motherboard. It connects internally to the logic output of the DUT (and the associated ground). This is the output that is normally monitored for “glitches” caused by high dV/dt rates on the common mode voltage. It will mate directly to the Tektronix P6246 differential probe, or to standard 0.1” header sockets. When using the differential probe, install the probe so that the “-” side is on the left, and the “+” side is on the right. A differential probe is used to help eliminate noise coupled from the high-voltage signals. Please note that the P6246 has a maximum differential input voltage range of 7V. If higher values of VCC2 are used, a different probe will be required. The “A” connector is active for both polarities. Since it is mounted on the motherboard, it is affected by the small parasitic inductance in the socketing arrangement. In demanding test scenarios, it may be preferable to connect to probe points on the daughterboard instead. “B” and “C” are provided for this purpose.

“B” provides access to the two-pin header connector mounted on the daughterboard, when the daughterboard is installed in the positive orientation.

“C” provides access to the two-pin header connector mounted on the daughterboard, when the daughterboard is installed in the negative orientation.

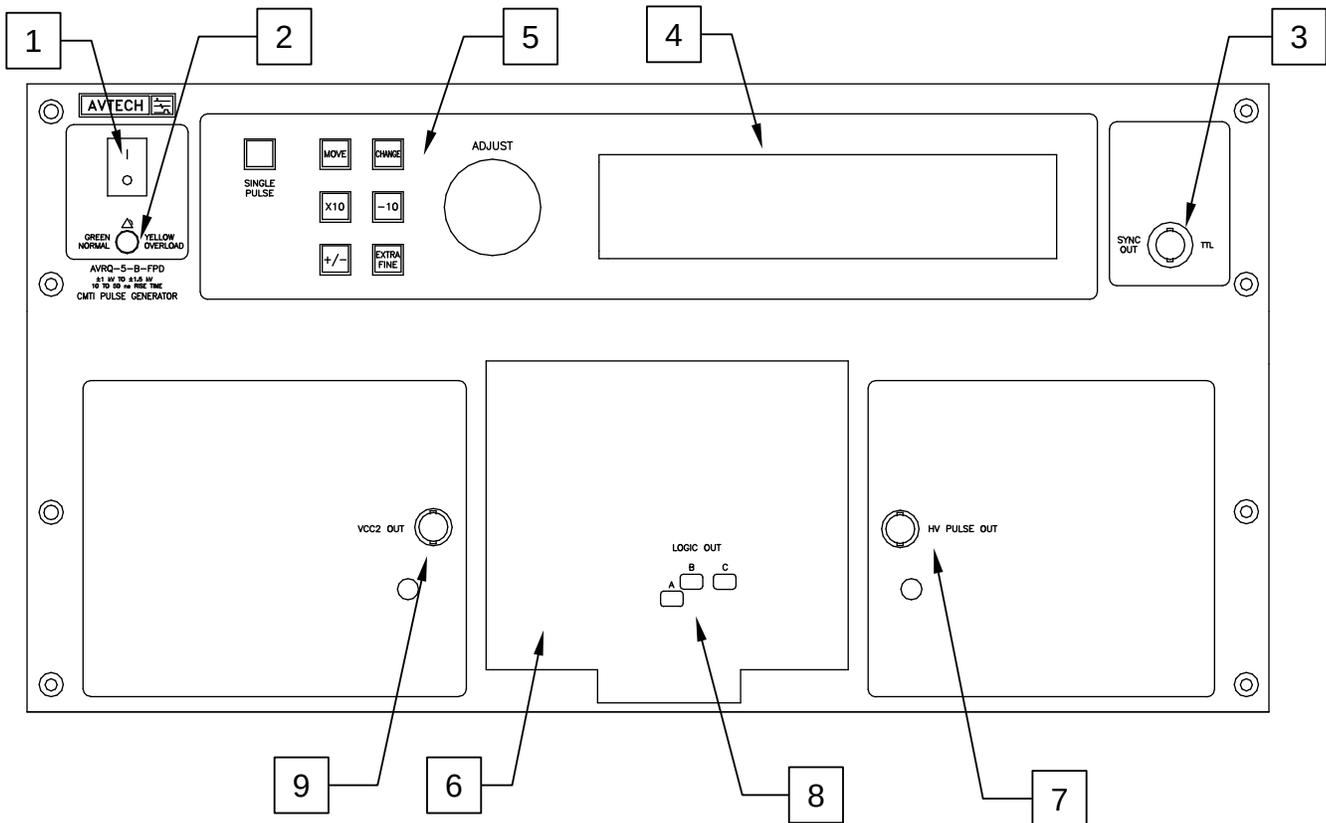
By default, the sample daughterboards as shipped from the factory do not have the two-pin headers connected to any signals. They must be configured with appropriate resistors and/or capacitors to enable this mode of operation. The B/C connector can be configured with resistive divider circuits on the daughterboard, allowing a low-voltage differential probe (like the P6246) to be used with a higher VCC2.

It is best to avoid measuring the low-voltage LOGIC OUT signal at the same time as a probe is connected to the HV PULSE signal. Inter-channel interference in the probes and oscilloscope may introduce significant noise on the low-voltage signal. Instead, measure the signals separately, and use the memory storage function of the oscilloscope if you wish to combine the signals on a single image.

12. VCC2 OUT Connector. (Optional feature. Present on units with the -V2 option only.) This output is wired in parallel with the VCC2 connection on the DUT socket, and may be used for monitoring purposes.



## FRONT PANEL CONTROLS (UNITS WITH -FPD OPTION)



1. **POWER Switch**. This is the main power switch. When turning the instrument on, there is normally a delay of 10 seconds before anything is shown on the main display, as the internal operating system boots up.
2. **OVERLOAD Indicator**. When the instrument is powered, this indicator is normally green, indicating normal operation. If this indicator is yellow, an internal automatic overload protection circuit has been tripped. If the unit is overloaded (by operating at an exceedingly high duty cycle or by operating into a very low impedance), the protective circuit will disable the output of the instrument and turn the indicator light yellow. The light will stay yellow (i.e. output disabled) for about 5 seconds after which the instrument will attempt to re-enable the output (i.e. light green) for about 1 second. If the overload condition persists, the output will be disabled again (i.e. light yellow) for another 5 seconds. If the overload condition has been removed, the instrument will resume normal operation.

This overload indicator may flash yellow briefly at start-up. This is not a cause for concern.

3. SYNC OUT. This connector supplies a SYNC output that can be used to trigger other equipment, particularly oscilloscopes. This signal leads (or lags) the main output by a duration set by the "DELAY" controls and has an approximate amplitude of +3 Volts to  $R_L > 1 \text{ k}\Omega$  with a pulse width of approximately 100 ns.
4. LIQUID CRYSTAL DISPLAY (LCD). This LCD is used in conjunction with the keypad to change the instrument settings. Normally, the main menu is displayed, which lists the key adjustable parameters and their current values. The "Programming Manual for -B Instruments" describes the menus and submenus in detail.
5. KEYPAD.

Control Name	Function
MOVE	This moves the arrow pointer on the display.
CHANGE	This is used to enter the submenu, or to select the operating mode, pointed to by the arrow pointer.
×10	If one of the adjustable numeric parameters is displayed, this increases the setting by a factor of ten.
÷10	If one of the adjustable numeric parameters is displayed, this decreases the setting by a factor of ten.
+/-	If one of the adjustable numeric parameters is displayed, and this parameter can be both positive or negative, this changes the sign of the parameter.
EXTRA FINE	This changes the step size of the ADJUST knob. In the extra-fine mode, the step size is twenty times finer than in the normal mode. This button switches between the two step sizes.
ADJUST	This large knob adjusts the value of any displayed numeric adjustable values, such as frequency, pulse width, etc. The adjust step size is set by the "EXTRA FINE" button.  When the main menu is displayed, this knob can be used to move the arrow pointer.

6. DUT Door. This is the door that provides access to the DUT socket. To open it, pull on the chrome knob. When closed, the door is held latched in place magnetically.

The high voltage output is automatically disabled when the DUT door is opened. The door must be closed during tests.

7. HV PULSE OUT CONNECTOR. The BNC connector provides access to the high voltage (up to  $\pm 2 \text{ kV}$ ) pulse that is applied to the DUT, for monitoring purposes. This signal must be observed on an oscilloscope to accurately measure the  $dV/dt$  rate of the high voltage pulse.

A Tektronix P5100 high-voltage probe with the 013-0291-00 probe-tip-to-BNC adapter, or a similar arrangement, should be used to connect to this output.

 CAUTION: Voltages as high as 2 kV may be present on the center conductor of this output connector. Avoid touching this conductor. Connect to this connector using a Tektronix P5100 high-voltage probe with the 013-0291-00 probe-tip-to-BNC adapter, or a similar arrangement, to ensure that the center conductor is not exposed.

 DO NOT CONNECT THIS OUTPUT DIRECTLY TO AN OSCILLOSCOPE. The oscilloscope will be damaged by the high voltages. Use a Tektronix P5100 high-voltage probe with the 013-0291-00 probe-tip-to-BNC adapter, or a similar arrangement.

 DO NOT CONNECT COAXIAL CABLING TO THIS OUTPUT. The capacitance of the cabling will reduce the dV/dt rates noticeably.

8. LOGIC OUT Connectors. There are three possible positions where the logic probe can be connected, “A”, “B”, and “C”.

“A” is a two-pin header connector mounted on the motherboard. It connects internally to the logic output of the DUT (and the associated ground). This is the output that is normally monitored for “glitches” caused by high dV/dt rates on the common mode voltage. It will mate directly to the Tektronix P6246 differential probe, or to standard 0.1” header sockets. When using the differential probe, install the probe so that the “-” side is on the left, and the “+” side is on the right. A differential probe is used to help eliminate noise coupled from the high-voltage signals. Please note that the P6246 has a maximum differential input voltage range of 7V. If higher values of VCC2 are used, a different probe will be required. The “A” connector is active for both polarities. Since it is mounted on the motherboard, it is affected by the small parasitic inductance in the socketing arrangement. In demanding test scenarios, it may be preferable to connect to probe points on the daughterboard instead. “B” and “C” are provided for this purpose.

“B” provides access to the two-pin header connector mounted on the daughterboard, when the daughterboard is installed in the positive orientation.

“C” provides access to the two-pin header connector mounted on the daughterboard, when the daughterboard is installed in the negative orientation.

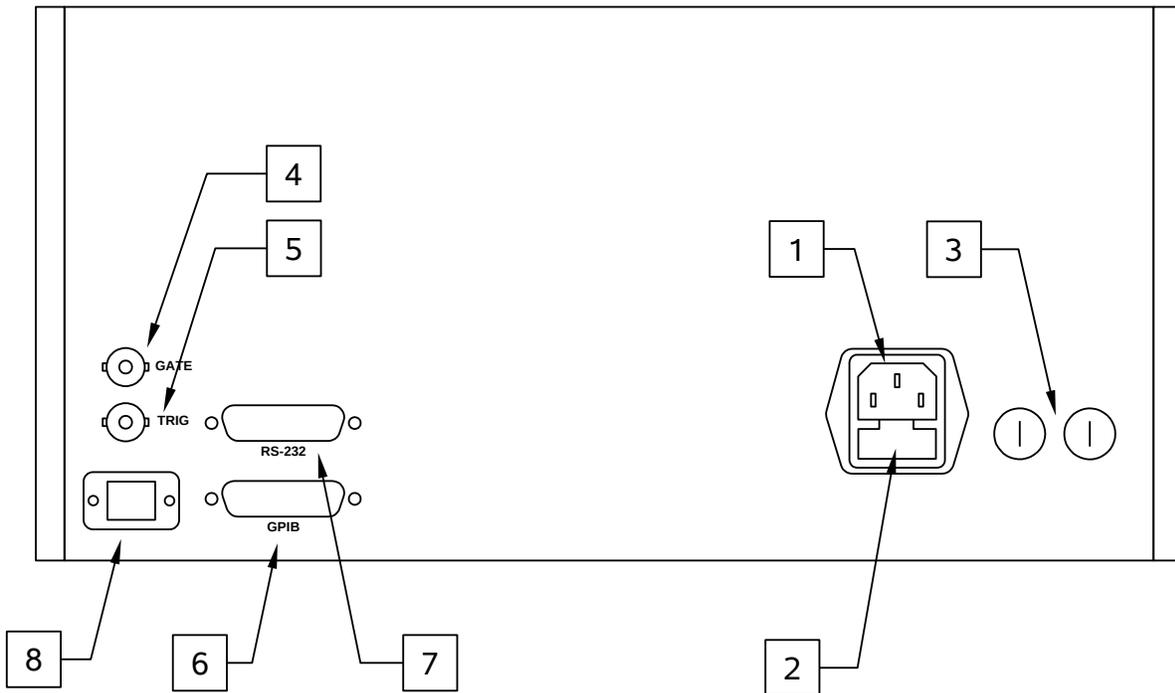
By default, the sample daughterboards as shipped from the factory do not have the two-pin headers connected to any signals. They must be configured with appropriate resistors and/or capacitors to enable this mode of operation. The B/C connector can be configured with resistive divider circuits on the daughterboard, allowing a low-voltage differential probe (like the P6246) to be used with a higher VCC2.

It is best to avoid measuring the low-voltage LOGIC OUT signal at the same time as a probe is connected to the HV PULSE signal. Inter-channel interference in the probes and oscilloscope may introduce significant noise on the low-voltage signal. Instead, measure the signals separately, and use the memory storage function of the

oscilloscope if you wish to combine the signals on a single image.

9. VCC2 OUT Connector. (Optional feature. Present on units with the -V2 option only.)  
This output is wired in parallel with the VCC2 connection on the DUT socket, and may be used for monitoring purposes.

## REAR PANEL CONTROLS (UNITS WITH -FPD OPTION)



*Note: some connectors may be in different positions than shown above, depending on the exact combination of options ordered.*

1. AC POWER INPUT. An IEC-320 C14 three-pronged recessed male socket is provided on the back panel for AC power connection to the instrument. One end of the detachable power cord that is supplied with the instrument plugs into this socket.
2. AC FUSE DRAWER. The two fuses that protect the AC input are located in this drawer. Please see the “FUSES” section of this manual for more information.
3. DC FUSES. These two fuses protect the internal DC power supplies. Please see the “FUSES” sections of this manual for more information.
4. GATE. This TTL-level (0 and +5V) logic input can be used to gate the triggering of the instrument. This input can be either active high or active low, depending on the front panel settings or programming commands. (The instrument triggers normally when this input is unconnected). When set to active high mode, this input is pulled-down to ground by a 1 k $\Omega$  resistor. When set to active low mode, this input is pulled-up to +5V by a 1 k $\Omega$  resistor.
5. TRIG. This TTL-level (0 and +5V) logic input can be used to trigger the instrument, if the instrument is set to triggering externally. The instrument triggers on the rising

edge of this input. The input impedance of this input is 1 k $\Omega$ . (Depending on the length of cable attached to this input, and the source driving it, it may be desirable to add a coaxial 50 Ohm terminator to this input to provide a proper transmission line termination. The Pasternack ([www.pasternack.com](http://www.pasternack.com)) PE6008-50 BNC feed-thru 50 Ohm terminator is suggested for this purpose.)

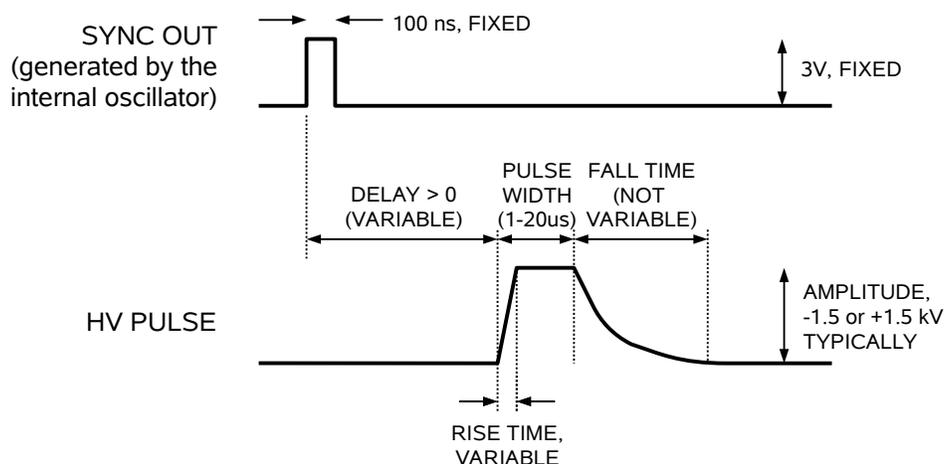
6.  GPIB Connector. A standard GPIB cable can be attached to this connector to allow the instrument to be computer-controlled. See the “Programming Manual for -B Instruments” for more details on GPIB control.
7.  RS-232 Connector. A standard serial cable with a 25-pin male connector can be attached to this connector to allow the instrument to be computer-controlled. A user name (“admin”) and a password (“default”, as shipped from the factory) are required when logging into a serial terminal session. The internal controller attempts to auto-sense the parity setting. It may be necessary to send a few return characters before attempting a login in order to provide enough data to allow this auto-sensing to work. (A standard Linux “agetty” process is used to implement serial control internally.) See the “Programming Manual for -B Instruments” for more details on RS-232 control.
8.  Network Connector. This Ethernet connector allows the instrument to be remotely controlled using the VXI-11.3, ssh (secure shell), telnet, and http (web) protocols. See the “Programming Manual for -B Instruments” for more details.

## GENERAL INFORMATION

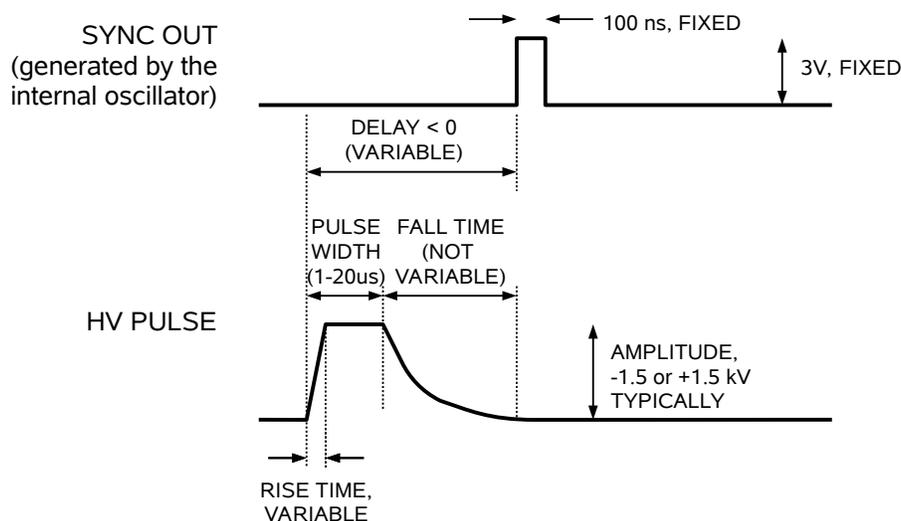
### BASIC PULSE CONTROL

This instrument can be triggered by its own internal clock or by an external TTL trigger signal. In either case, two output channels respond to the trigger: HV PULSE and SYNC. The HV PULSE channel is the signal that is applied to the DUT. The SYNC pulse is a fixed-width TTL-level reference pulse used to trigger oscilloscopes or other measurement systems. When the delay is set to a positive value the SYNC pulse precedes the HV PULSE pulse. When the delay is set to a negative value the SYNC pulse follows the HV PULSE pulse.

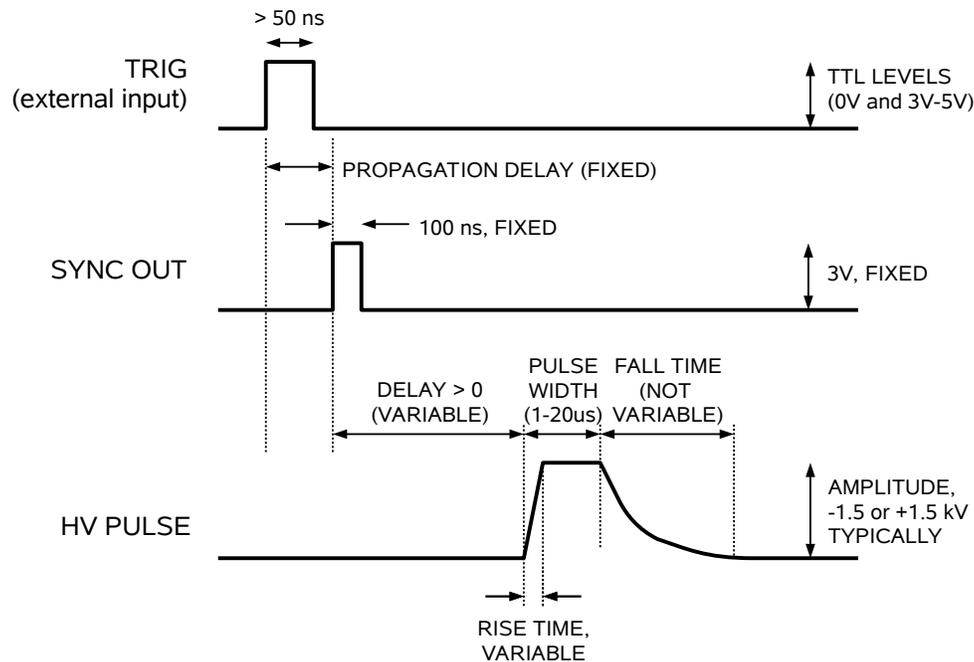
These pulses are illustrated below, assuming internal triggering, a positive delay, and positive amplitude:



If the delay is negative, the order of the SYNC and OUT pulses is reversed:



The next figure illustrates the relationship between the signals when an external TTL-level trigger is used:



As before, if the delay is negative, the order of the SYNC and OUT pulses is reversed.

The delay and frequency (when in the internal mode), of the OUT pulse can be varied with front panel controls or via the GPIB or RS-232 computer interfaces.

## TRIGGER MODES

This instrument has four trigger modes:

- Internal Trigger: the instrument controls the trigger frequency, and generates the clock internally.
- External Trigger: the instrument is triggered by an external TTL-level clock on the back-panel TRIG connector.
- Manual Trigger: the instrument is triggered by the front-panel "SINGLE PULSE" pushbutton.
- Hold Trigger: the instrument is set to not trigger at all.

These modes can be selected using the front panel trigger menu, or by using the appropriate programming commands. (See the “Programming Manual for -B Instruments” for more details.)

### GATING MODES

Triggering can be suppressed by a TTL-level signal on the rear-panel GATE connector. The instrument can be set to stop triggering when this input high or low, using the front-panel gate menu or the appropriate programming commands. This input can also be set to act synchronously or asynchronously. When set to asynchronous mode, the GATE will disable the output immediately. Output pulses may be truncated. When set to synchronous mode, the output will complete the full pulse width if the output is high, and then stop triggering. No pulses are truncated in this mode.



## DUT INSTALLATION

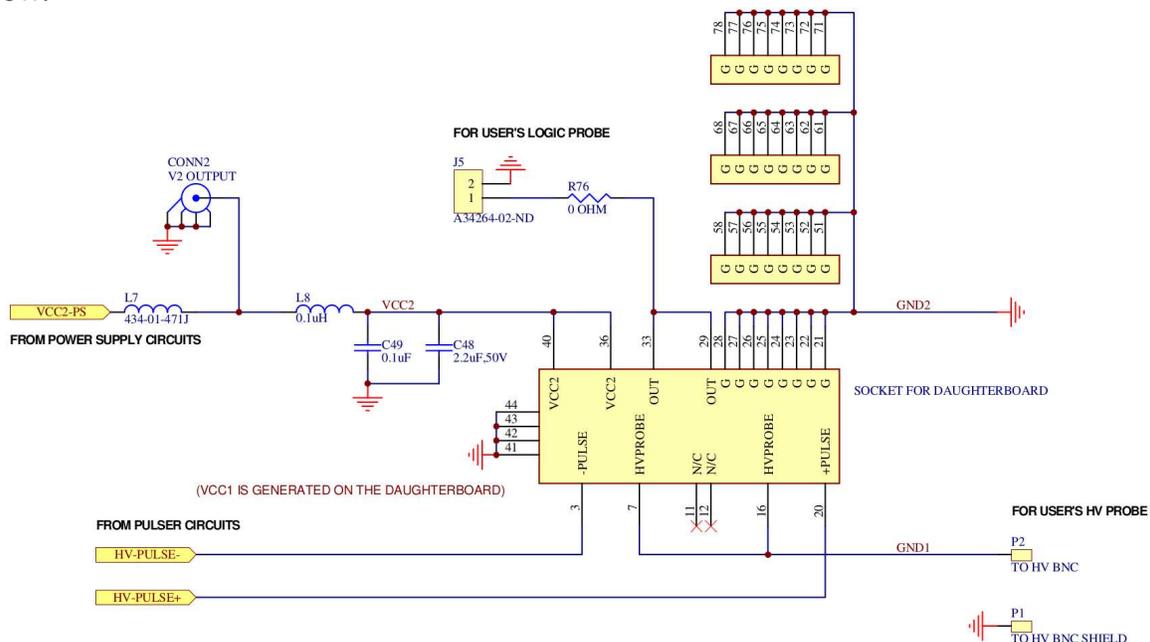
### SOCKET PINOUT

A daughterboard arrangement is used to accommodate difference device packages and bias conditions. An arrangement of pin sockets on the main motherboard accepts these daughterboards.

The AVRQ-5-B mainframe provides the high-voltage common mode pulse (which is tied to GND1), and VCC2 / GND2 (the non-floating output-side power supply). The user is responsible for configuring the daughterboards to implement the correct input side power (VCC1), biasing, filtering, loading, socketing, and glitch measurement. The included sample boards implement these requirements for common DIP8 devices, using configurable jumpers/resistors/capacitors. A probe point is provided on the motherboard for observation of the device logic output with a user-provided probe and oscilloscope. An optional probe point is also provided on the sample daughterboards.

The ground-referenced output-side power (VCC2) is generated by the mainframe, and is adjustable (+3V to +43V, 150 mA maximum). The floating input-side power is not provided by the mainframe. Instead, an A23-type 12V battery should be installed on the DUT daughterboard to provide a floating power source, along with a basic regulator circuit to provide the necessary regulated +5V power (VCC1). A isolated battery arrangement is used to ensure that the VCC1 power supply is not the source of any glitches observed in the operation of the DUT.

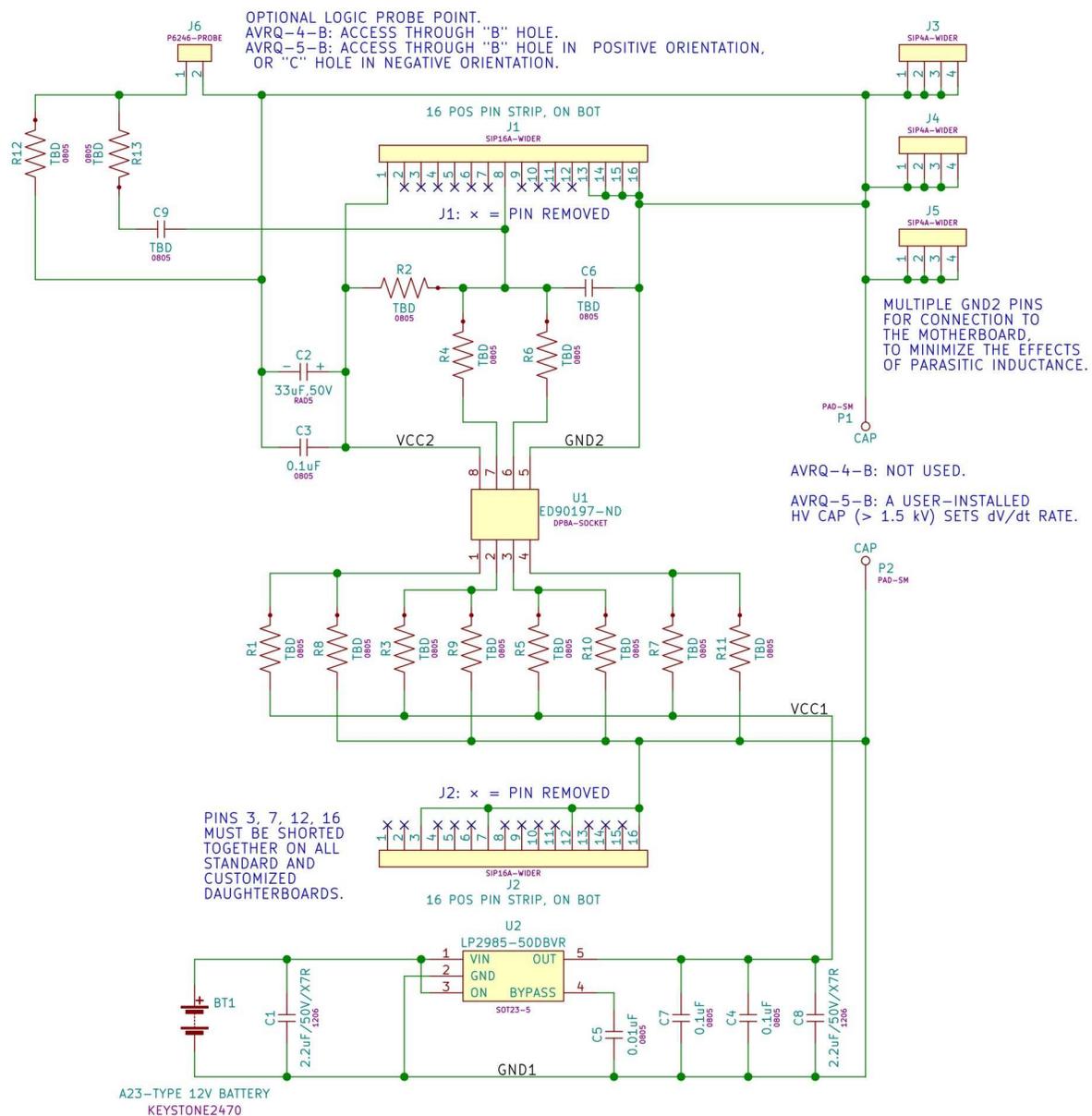
The AVRQ-5-B provides a pin socket arrangement into which the daughterboard may be plugged. The simplified circuit diagram of the socketing on the mainframe is shown below:



The socket and the sample daughterboards are designed so that the daughterboard can be installed in two positions – one for positive pulse mode, and one for negative pulse mode. Two physical positions are used to achieve polarity switching, rather than using internal high-voltage relays, in order to achieve the fastest possible switching times. The parasitic inductance and capacitance added by physically-large high-voltage relays would degrade performance noticeably. The front-panel AMP1 setting determines which of the two internal pulse generator circuits (+ and -) is active. Only one is active at a time, to avoid interference.

## DAUGHTERBOARD PINOUT

The sample daughterboards have the pinout shown below:



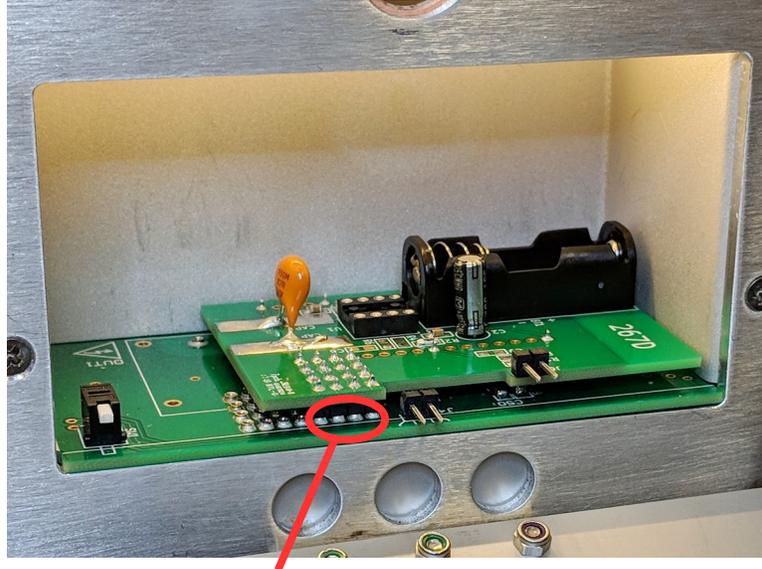
For positive pulse mode, the “AMP1” front-panel setting must be set to a positive value *AND* the daughterboard must be installed in the socket so that it is in the left-most position (when viewed from the DUT area door opening), like this:



The left-most four GND2 pin sockets are used in the positive orientation.

### ***DAUGHTERBOARD INSTALLED FOR POSITIVE PULSE OPERATION***

For negative pulse mode, the “AMP1” front-panel setting must be set to a negative value *AND* the daughterboard must be installed in the socket so that it is in the right-most position (when viewed from the DUT area door opening), like this:



The right-most four GND2 pin sockets are used in the negative orientation.

### ***DAUGHTERBOARD INSTALLED FOR NEGATIVE PULSE OPERATION***

**⚠** THESE ARE THE ONLY TWO CORRECT POSITIONS. THE BOARDS WILL NOT MATE IN ANY OTHER CONFIGURATION.

Two circuit diagrams in the BASIC TEST ARRANGEMENTS section (page 53) show how the socket and daughterboard pins mesh in the two polarity configurations, electrically.

### **DAUGHTERBOARD COMPONENTS**

The circuit diagram for the included sample daughterboards shown on page 44 includes more than just the socket for the 8-pin DUT.

A battery holder (BT1) is provided to hold one A23-type 12V battery. When installed by the user, this battery will apply +12V to the regulator IC (U2), which provides a floating +5.0V power source (VCC1) to the DUT. An A23 battery is supplied with each sample daughterboard, and additional ones can be easily purchased from Digi-Key (see stock number N403-ND, [www.digikey.com/product-detail/en/A23C/N403-ND](http://www.digikey.com/product-detail/en/A23C/N403-ND)). The battery is not required if the DUT does not require a voltage or current bias (for example, when testing current-drive opto-couplers in the LED “off” state).

A number of bypass capacitors are installed by default.

Two resistor footprints are associated with each of pins 1 – 4 of the DUT, allowing these pins to be individually tied to VCC1, GND1, or be left open.

Resistor footprints R4 and R6 allow either pin 6 or 7 (or both) of the DUT to be used as the logic output. R2 can be used to pull-up the DUT output (if it is an open-collector output, in particular) and C6 can be used to add a load capacitance to the logic output. These component values are sometimes specified by particular test standards.

⚠ The user will need to configure R1-R11 and C6 as appropriate for the DUT.

Two solder pads (P1 and P2 in the schematic, both are labeled “CAP” on the actual PCB) are also provided. A high-voltage ceramic capacitor (rated for at least 2 kV) may be soldered between these two pads in order to increase the rise time of the pulse. With no capacitance installed, switching times of < 10 ns (10%-90%) are normally obtainable.

⚠ Do not exceed 600 pF on standard units, or 1200 pF on -XHV units, or the switching transistors may become overstressed and fail.

Lastly, components C9, R12, R13 and J6 provide an optional logic probe point on the daughterboard. J6 is installed by default (as shipped from the factory), but C9, R12, and R13 are not. If a direct connection is desired from the DUT logic output to J6, then zero Ohm jumpers can be installed in the C9 and R13 positions. R12 and R13 can also be used to implement a resistive divider, if it is necessary to reduce the amplitude of a high-voltage logic signal so that a low-voltage differential probe can be used. C9 may be used to provide AC-coupling, if desired. The exact implementation of this optional circuitry is up to the user. J6 is accessed through the LOGIC OUT “B” hole on the DUT door when the daughterboard is installed in the positive orientation. J6 is accessed through the LOGIC OUT “C” hole on the DUT door when the daughterboard is installed in the negative orientation. The LOGIC OUT “A” connector remains active regardless of the use of J6.

The design files for the sample daughterboard (Avtech PCB 267D) are available for download at [https://www.avtechpulse.com/semiconductor/avrq-5/#support\\_files](https://www.avtechpulse.com/semiconductor/avrq-5/#support_files).

The function of the various components is summarized below:

Reference	Footprint	Installed Value	Normally Modified by User	Typical Function
C1	1206	2.2uF,50V,X7R	No	VCC1 decoupling
C2	RAD5	33uF,50V		VCC2 decoupling
C3	0805	0.1uF		VCC2 decoupling
C4	0805	0.1uF		VCC1 decoupling
C5	0805	0.01uF		VCC1 decoupling
C7	0805	0.1uF		VCC1 decoupling
C8	1206	2.2uF,50V,X7R		VCC1 decoupling
U1	DP8A-SOCKET	DIP8 SOCKET		DUT socket
J1	SIP16A-WIDER	CONN16		Mates with socketing, some pins removed
J2	SIP16A-WIDER	CONN16		Mates with socketing, some pins removed
J3	SIP4A-WIDER	CONN4		Mates with socketing
J4	SIP4A-WIDER	CONN4		Mates with socketing

J5	SIP4A-WIDER	CONN4		Mates with socketing
U2	SOT23-5	LP2985-50DBVR		Low-dropout 5V regulator VCC1
C6	0805	-	Yes	Load capacitance
R1		-		Zero-Ohm Jumper to connect DUT pin 1 to VCC1
R2		-		Output pullup
R3		-		Resistance to connect DUT pin 2 to VCC1. Non-zero resistance for current-drive inputs.
R4		-		Zero-Ohm Jumper for DUT pin 7 as logic output
R5		-		Resistance to connect DUT pin 3 to VCC1
R6		-		Zero-Ohm Jumper for DUT pin 6 as logic output
R7		-		Resistance to connect DUT pin 4 to VCC1
R8		-		Zero-Ohm Jumper to connect DUT pin 1 to GND1
R9		-		Zero-Ohm Jumper to connect DUT pin 2 to GND1
R10		-		Zero-Ohm Jumper to connect DUT pin 3 to GND1
R11	-	Zero-Ohm Jumper to connect DUT pin 4 to GND1		
P1	PAD-SM	-		Pads for rise time capacitor. Do not exceed 600 pF.
P2		-		
BT1	KEYSTONE2470	-		One user-installed A23-type 12V battery, prime power for VCC1. (Please note that A23 batteries have a limited mA·hr rating – typically 30 mA·hr when operating at 15 mA – so the battery should be removed immediately after testing, and its output should be verified to be between 6V and 12V before each test.)
J6	P6246-PROBE	A34264-02-ND	No	Optional logic probe point circuit
C9	0805	-	Optional	
R12		-		
R13		-		

### SO-8 DAUGHTERBOARD (PCB 314B)

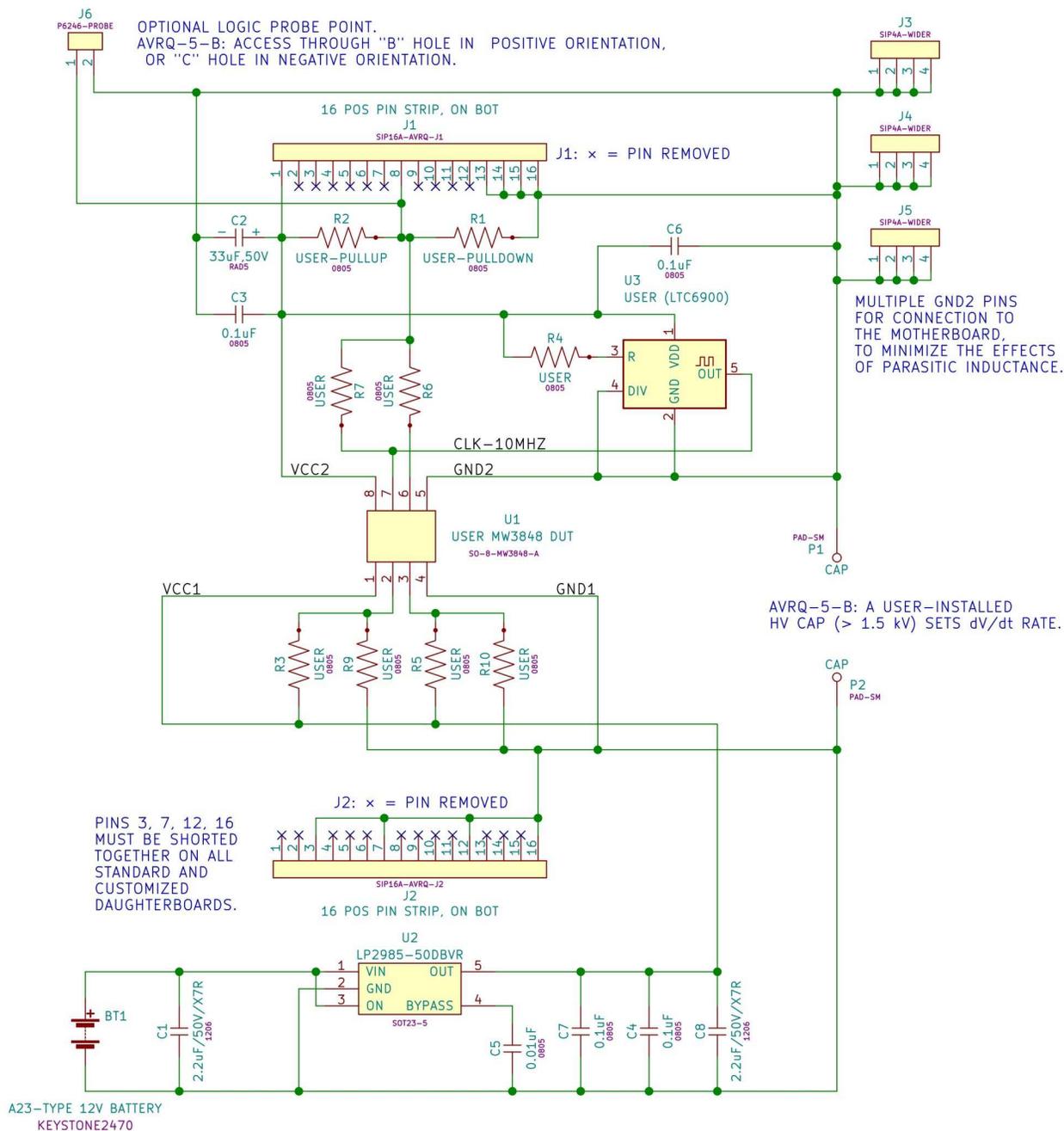
Units with the -SO8 option are provided with 32 additional unpopulated (bare) daughterboards (PCB 314B), suitable for use with standard SO-8 packages. These PCBs require assembly.

These PCBs are essentially identical to PCB 267D described in the previous section, except that the 8-pin DIP socket is replaced with a footprint for an SO-8 package. The user will need to solder the devices directly to the PCB, limiting the number of times that each PCB and device can be used. CAM files are available, so that the user may produce additional daughterboards as required:

[https://www.avtechpulse.com/semiconductor/avrq-4/#support\\_files](https://www.avtechpulse.com/semiconductor/avrq-4/#support_files)

## CUSTOMER-SPECIFIC PCB 324B DAUGHTERBOARD

PCB 324B is a special-order daughterboard with the following circuitry:



Its operation is similar to that of the standard daughterboard, except that provision has been added for a user-configurable output-side oscillator.

## CUSTOM DAUGHTERBOARDS

The daughterboards provided with the AVRQ-5-B are meant as samples.

The user may construct their own daughterboards, which may incorporate a preferred physical layout, different bias circuits, or different DUT packages and socketing.

 When designing your own daughterboard, take care to isolate the input and output sides as much as possible, to both provide sufficient high-voltage clearance and to minimize parasitic coupling of the HV pulse onto the output signal.

 If the user designs a custom daughterboard, the same connections must be made to the pins of the daughterboard. That is, pins 3, 7, 12, and 16 on J1 (GND1) must be shorted together, VCC2 must go to J1:1, GND2 to J1:13-16 (and J3, J4, J5), and the logic output to J1:8.

The battery occupies a relatively large portion of the top side of the standard daughterboard. It may be necessary to locate the footprints for large SMT DUTs (e.g., 32-pin SOICs) on the bottom side of the PCB. It may also be possible to mount the battery vertically to provide more DUT space on the top side.

Do not use coin batteries to power the floating side of the DUT. They are normally severely restricted in their output current rating and can not supply the 2-20 mA typically required to power the floating side of the DUT, regardless of their mA·hr rating. The A23-style 12V battery has an appropriate combination of voltage output, current rating, and physical size.

The sample daughterboard uses a simple DIP socket for the DUT, rather than the more convenient ZIF-style of socket. This is done because ZIF sockets have higher parasitic capacitance between the various pins, which can be very harmful to the DUT's CMTI performance. Avoid ZIF sockets for the DUT.

## DIFFERENTIAL PROBING

The mainframe uses a two-pin header near the DUT area door to transmit the output waveform to a user-supplied Tektronix P6246 differential probe. The use of a differential probe helps reduce spurious transient signal artefacts on the oscilloscope, which are typically caused by ground bounce and interference in general.

When designing custom daughterboards, a similar approach should be used.

Please note that the P6246 has a maximum differential input voltage range of 7V. If higher values of VCC2 will be used, a different probe will be required. Other probes may be used by installing a matching two-pin socket as an extender.

## INSTALLING THE DAUGHTERBOARDS

To install a daughterboard, first turn off the instrument. (The instrument will disable the high-voltage circuitry automatically if the DUT door is opened, but it is better practice to turn off the instrument entirely.)

Install the desired 8-pin DIP device in the DIP socket on the loose daughterboard.

If necessary for input biasing and/or VCC1 generation, install an A23-type battery on the daughterboard. Confirm that it is generating >6V once it is installed in the battery holder.

Open the rear-panel DUT door.

Carefully lower the daughterboard into the left-most position (for positive tests) or the right-most position (for negative tests). Press the daughterboard into the socketing.

Close the DUT door. Turn on the instrument and proceed with your tests.

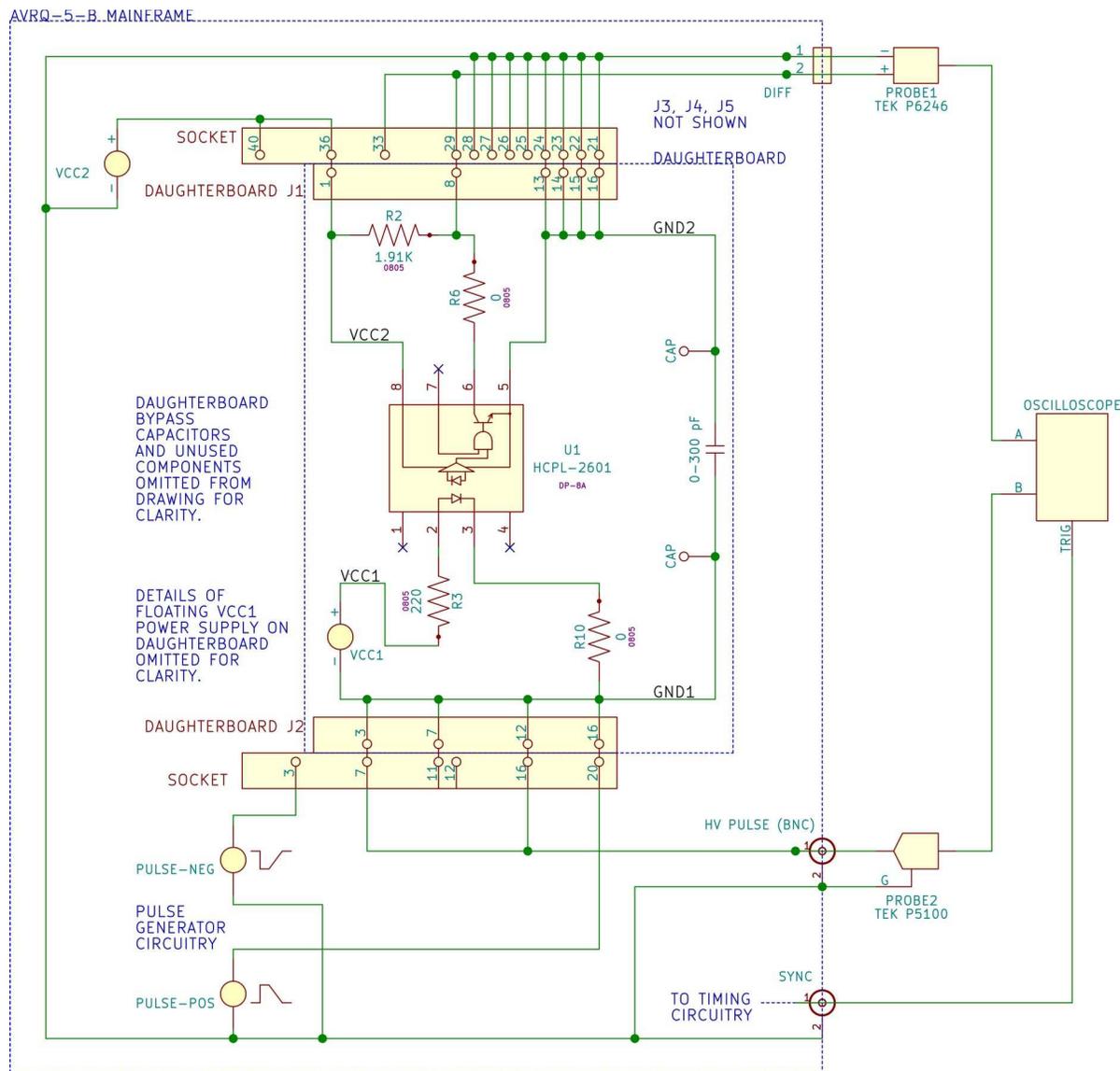
When testing is finished, turn off the instrument, open the DUT door, and gently pry the daughterboard up out of the socket.

Remove the DUT and A23-type battery, if used.



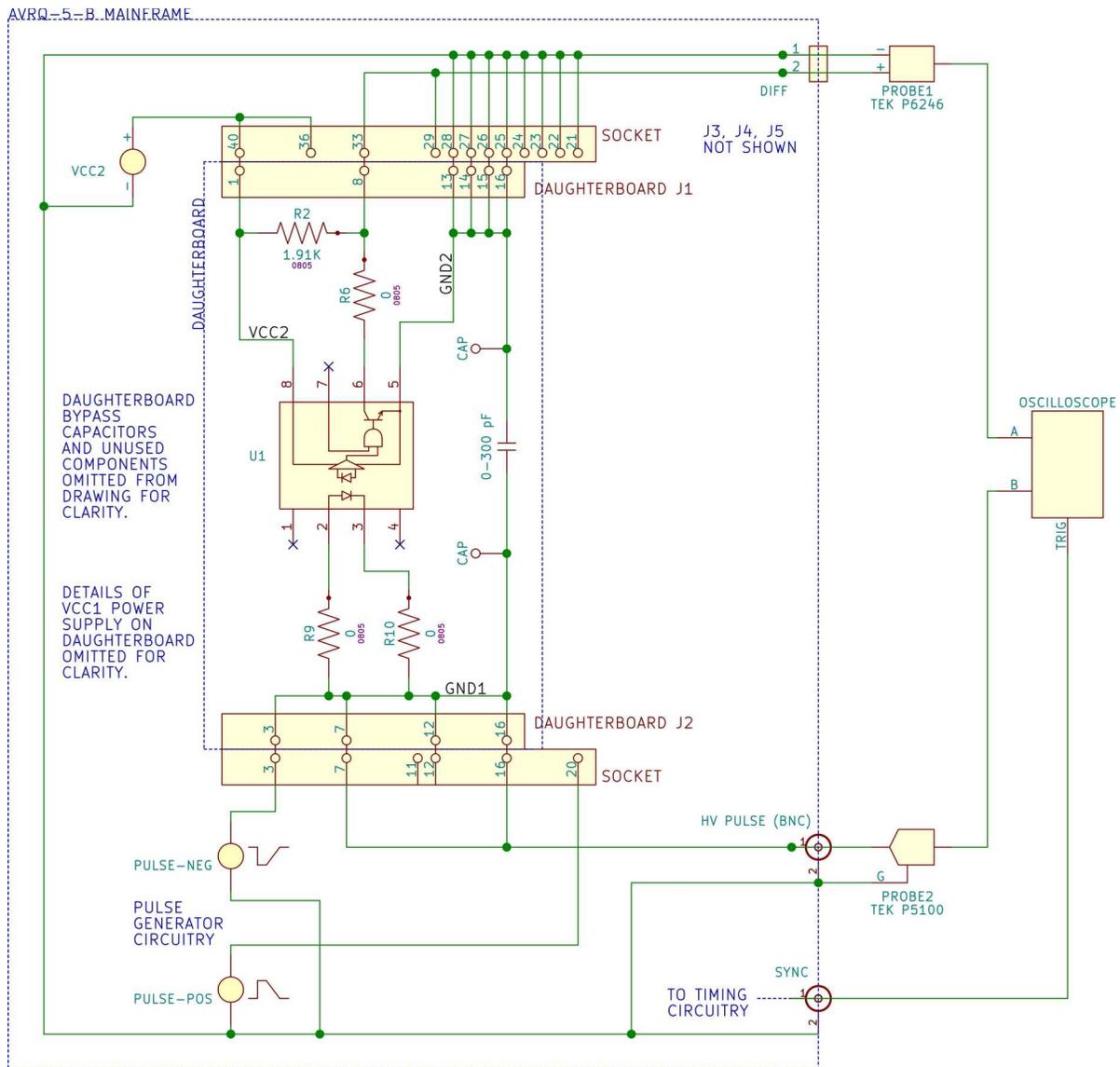
## BASIC TEST ARRANGEMENTS

The figure below shows the basic test arrangement for the AVRQ-5-B, with one possible DUT daughterboard configuration, with the daughterboard installed for positive pulse operation and a high-current input bias on the LED:



In the above drawing, an HCPL-2601 current-drive opto-coupler is installed on the daughterboard, and the daughterboard is configured to drive the opto-coupler input with  $\sim 16$  mA of current (using VCC1 and a 220 Ohm resistance). The daughterboard is positioned to connect the daughterboard to the positive pulse circuitry.

The figure below shows another basic test arrangement, with the daughterboard installed for negative pulse operation and zero input bias on the LED:



In the above drawing, an HCPL-2601 current-drive opto-coupler is installed on the daughterboard, and the daughterboard is configured to drive the opto-coupler input with zero current (by jumpering pins 2 and 3 to GND1). The daughterboard is positioned to connect the daughterboard to the negative pulse circuitry.

To connect the AVRQ-5-B properly, do the following:

- 1) With the power off, install an appropriately-configured daughterboard and DUT, as described in the previous sections.
- 2) Connect the SYNC output (on the front panel) to the external trigger input of the oscilloscope using (user-supplied) coaxial cabling.
- 3) Connect the (user-supplied) Tektronix P5100 probe to the rear-panel HV PULSE connector using the (user-supplied) Tektronix 013-0291-00 probe-to-BNC

adapter, or a similar arrangement.

- 4) With the DUT door closed, gently insert the Tektronix P6246 differential probe to mate with the output header on the daughterboard. When using the differential probe, install the probe so that the “-” side is on the left, and the “+” side is on the right. Please note that the P6246 has a maximum differential input voltage range of 7V. If higher values of VCC2 will be used, a different probe will be required.
- 5) Power-up the AVRQ-5-B and the oscilloscope.

 Caution: The HV PULSE oscilloscope probe must be rated for operation at 2 kV (pulsed) or higher. Factory tests are conducted using a Tektronix P5100 probe, which has a 2.5 kV peak rating and a 1000:1 division ratio. (Remember to adjust the compensation of the probe to match your oscilloscope input.)

### INTER-CHANNEL INTERFERENCE

The test arrangements on the preceding pages show both the high-voltage pulse and the logic output being measured on the oscilloscope at the same time.

In practice, better results are obtained if the logic waveform is measured with the high-voltage probe disconnected from the “HV PULSE” output. Otherwise, some of the very-fast, very-high-voltage signal may couple to the low-voltage logic input through parasitic capacitances in the oscilloscope and its cabling. This sort of interference is typically quite sensitive to the exact positioning of the probe cabling.

If you observe this sort of interference, measure the signals one at a time, and use the memory-storage feature of your oscilloscope if you wish to record them on the same waveform photo.



## TYPICAL WAVEFORMS FOR STANDARD DAUGHTERBOARDS

### BASIC THEORY

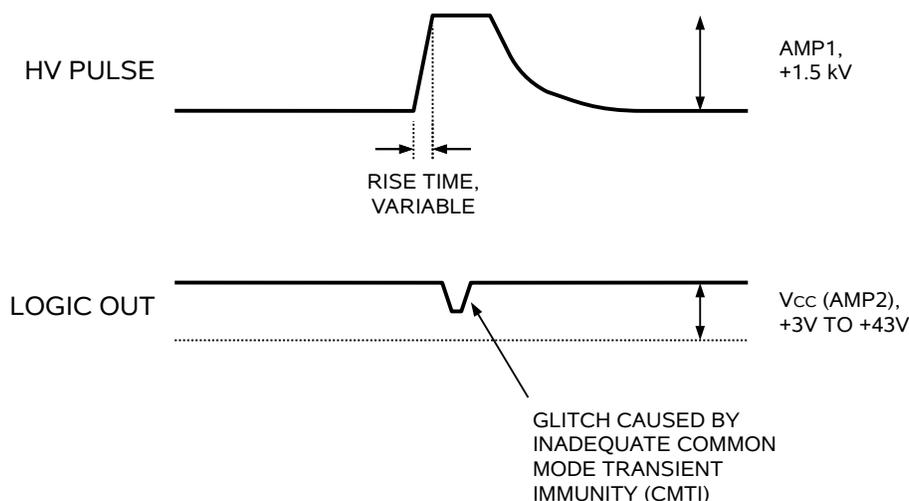
The user will install a DUT on a daughterboard. The daughterboard configuration determines the input bias to the opto-coupler, as well as the output loading.

The AVRQ-5-B front panel settings control whether the positive or negative pulse generator circuit is active internally. The daughterboard must be positioned in the socketing to match this setting.

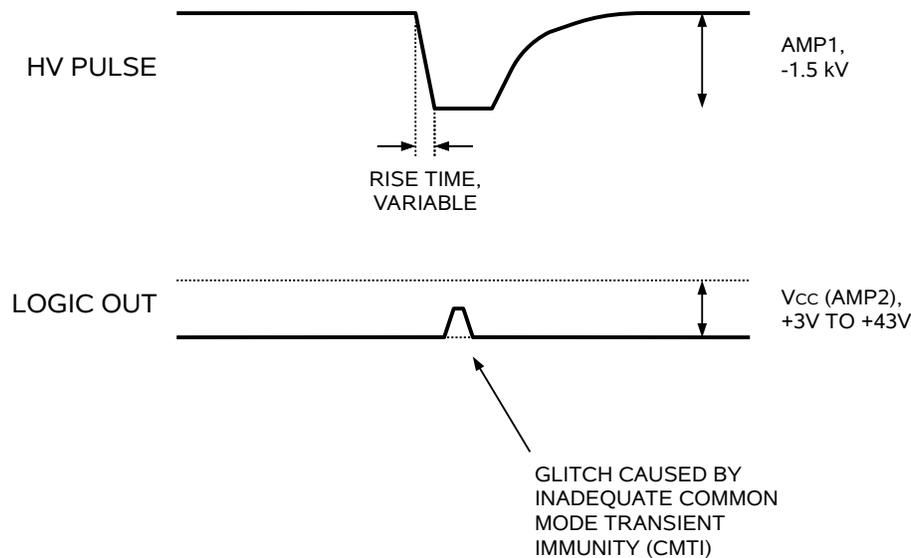
The AVRQ-5-B front panel settings also control the DC voltage applied to VCC2 (+3 to +43V, adjustable, 150 mA maximum). This is the opto-coupler output-side bias. GND2 is connected to chassis ground.

The opto-coupler input-side bias is controlled by the circuitry installed on the daughterboard, as explained in previous sections. If a non-zero voltage or current bias is required, then an A23-type 12V battery must be installed in the battery holder on the daughterboard. (Please note that A23 batteries have a limited mA·hr rating – typically 30 mA·hr when operating at 15 mA – so the battery should be removed immediately after testing, and its output should be verified to be between 6V and 12V before each test.)

As an example, the HV pulse might be set to a positive amplitude (+1.5 kV), with the input anode and cathode both connected to GND1 (zero current bias). In this mode, the output voltage should be pulled-up to VCC2. However, as the rise time of the HV pulse is reduced, the interference caused by the fast pulse may cause a “glitch” to appear on the output, where the output changes state (or come close to it). This is illustrated below:

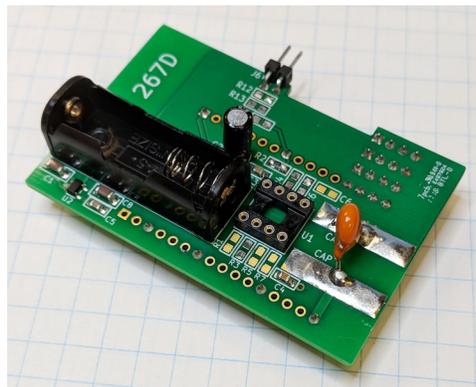


The next illustration shows a similar glitch occurring for a negative high-voltage pulse, where the input has been biased “on” to provide a normally-zero output voltage:



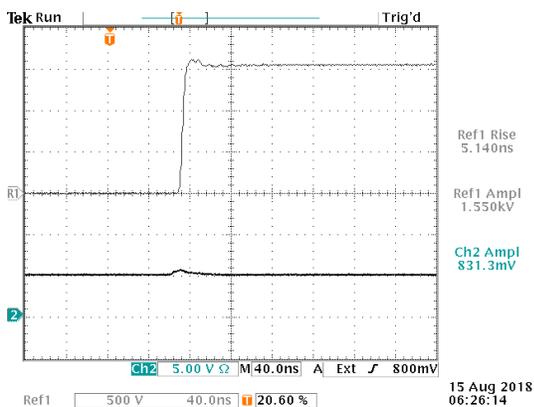
### CONTROLLING THE TRANSITION TIME

The positive and negative pulse generators in the AVRQ-5-B are essentially switched current sources. The voltage rise time can be controlled by deliberately soldering capacitance between the two “CAP” pads on the daughterboards (between the GND1 and GND2 signals). This capacitance should be added using high-voltage (> 2 kV) ceramic capacitors. Factory tests are conducted using Vishay Cera-Mite 564R-series capacitors, which are readily available for purchase from Digi-Key. Some of the tests below use series or parallel combinations of part number 564R30GAT15, which is a 150 pF / 3 kV capacitor. The photo below shows a 564R30GAT15 capacitor installed:

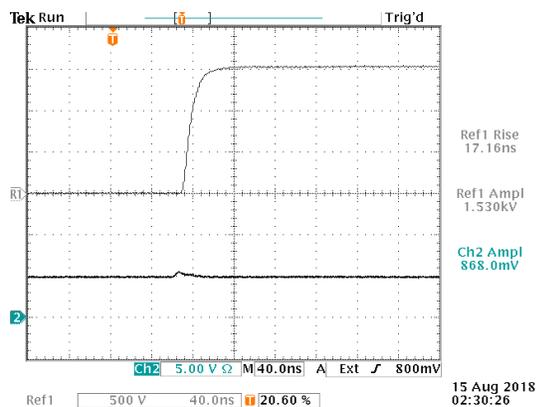


## TYPICAL POSITIVE RESULTS, WITH NO DUT INSTALLED

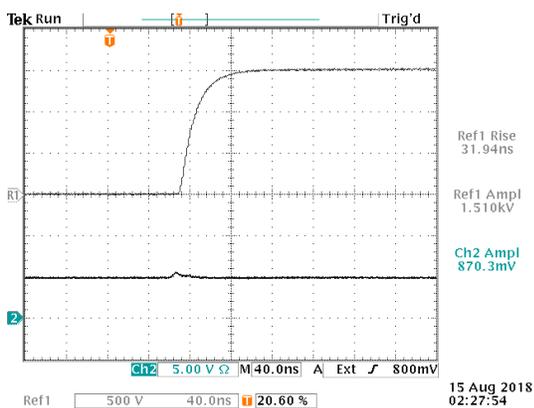
The photos below show typical “HV PULSE” waveforms with with AMP1 = +1.5 kV, and a daughterboard installed in the socketing in the positive position, but with no DUT installed in the DIP8 socket on the daughterboard. (The lower waveform in each photo is the LOGIC OUT “A” output, with R2 = 1 kΩ. A small signal is coupled through parasitic inductance/capacitance in the socketing.)



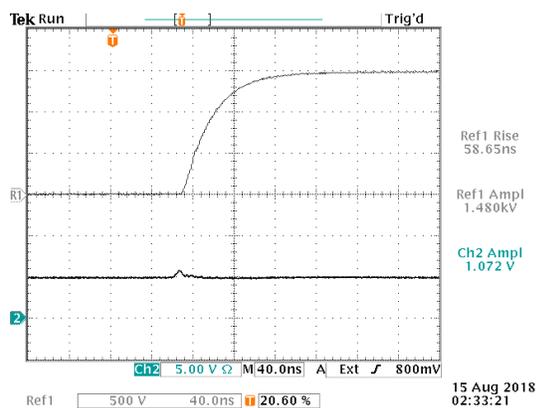
C = 0 pF,  $t_{R10-90}$  = 5.140 ns



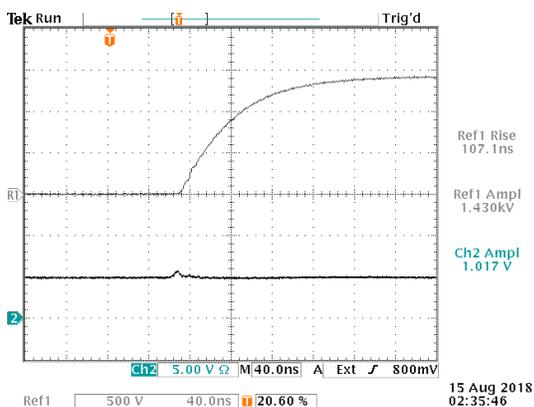
C = 75 pF,  $t_{R10-90}$  = 17.16 ns



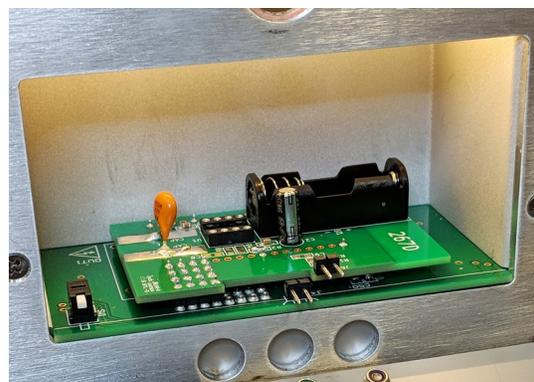
C = 150 pF,  $t_{R10-90}$  = 31.94 ns



C = 300 pF,  $t_{R10-90}$  = 58.65 ns



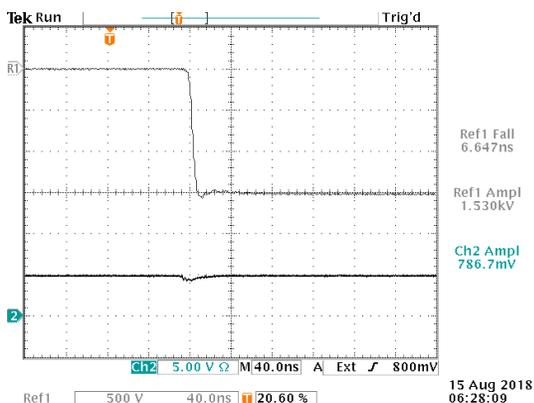
C = 600 pF,  $t_{R10-90}$  = 107.1 ns



Positive positioning  
of daughterboard

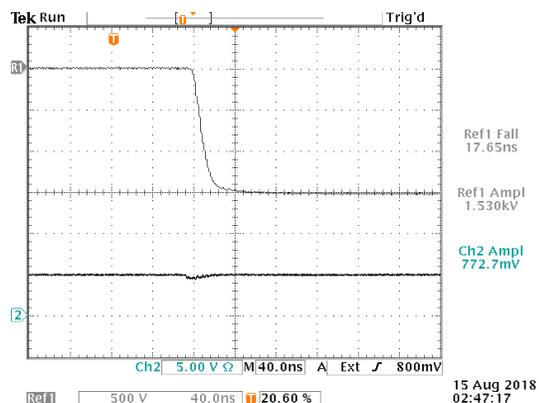
## TYPICAL NEGATIVE RESULTS, WITH NO DUT INSTALLED

The photos below show typical “HV PULSE” waveforms with with AMP1 = -1.5 kV, and a daughterboard installed in the socketing in the negative position, but with no DUT installed in the DIP8 socket on the daughterboard. (The lower waveform in each photo is the LOGIC OUT “A” output, with R2 = 1 kΩ. A small signal is coupled through parasitic inductance/capacitance in the socketing.)

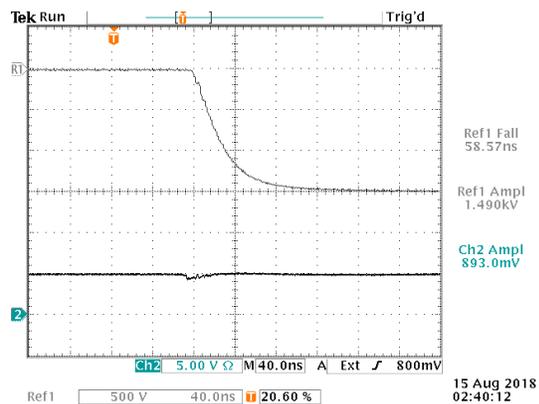


$C = 0 \text{ pF}$ ,  $t_{R10-90} = 6.647 \text{ ns}$

$C = 150 \text{ pF}$ ,  $t_{R10-90} = 33.33 \text{ ns}$

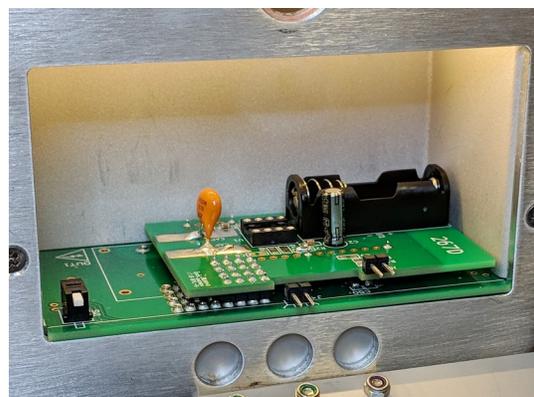


$C = 75 \text{ pF}$ ,  $t_{R10-90} = 17.65 \text{ ns}$



$C = 300 \text{ pF}$ ,  $t_{R10-90} = 58.57 \text{ ns}$

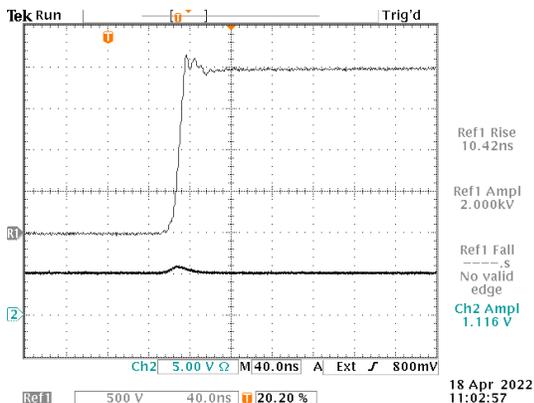
$C = 600 \text{ pF}$ ,  $t_{R10-90} = 100.8 \text{ ns}$



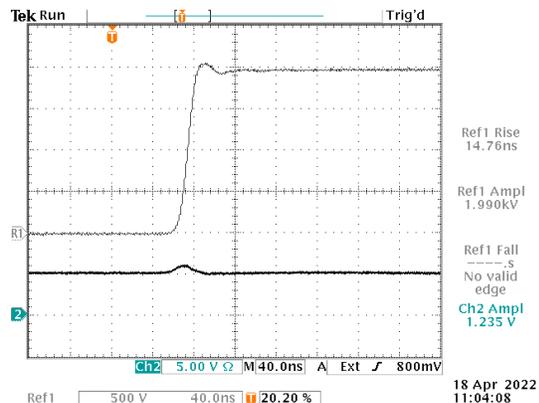
Negative positioning  
of daughterboard

## TYPICAL POSITIVE RESULTS (-XHV UNITS)

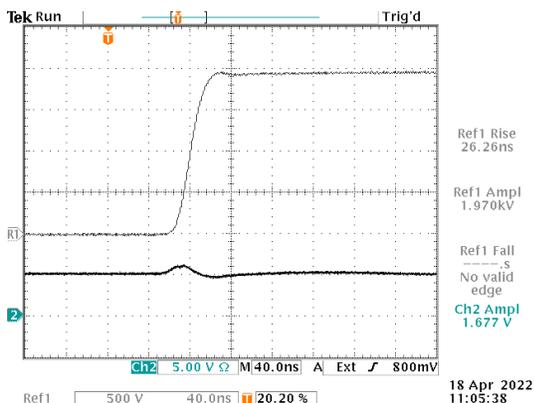
Units with the -XHV option can operate at higher amplitudes, up to 2 kV. The photos below show typical “HV PULSE” waveforms with with AMP1 = +2 kV, and a daughterboard installed in the socketing in the positive position, but with no DUT installed in the DIP8 socket on the daughterboard. (The lower waveform in each photo is the LOGIC OUT “A” output, with R2 = 1 kΩ. A small signal is coupled through parasitic inductance/capacitance in the socketing.)



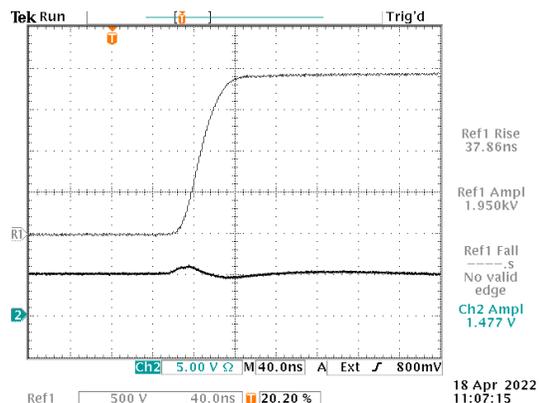
$C = 0 \text{ pF}$ ,  $t_{R10-90} = 10.42 \text{ ns}$



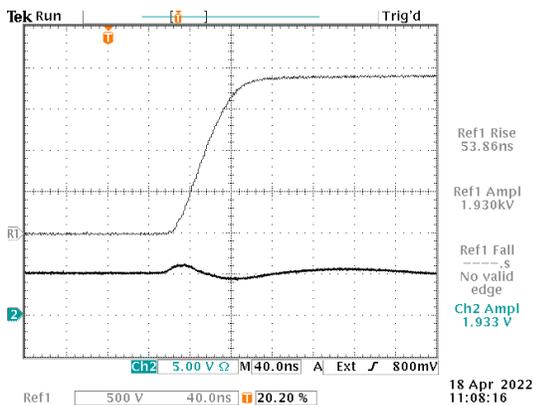
$C = 150 \text{ pF}$ ,  $t_{R10-90} = 14.76 \text{ ns}$



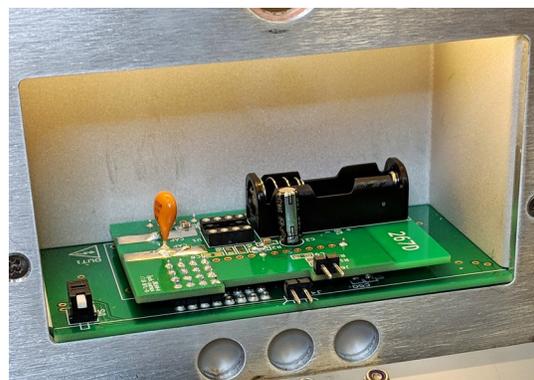
$C = 450 \text{ pF}$ ,  $t_{R10-90} = 26.26 \text{ ns}$



$C = 820 \text{ pF}$ ,  $t_{R10-90} = 37.86 \text{ ns}$



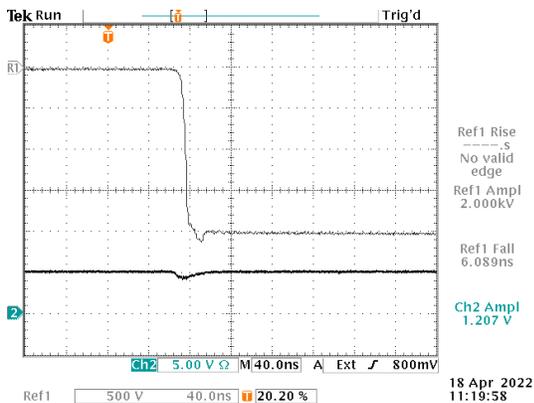
$C = 1000 \text{ pF}$ ,  $t_{R10-90} = 53.86 \text{ ns}$



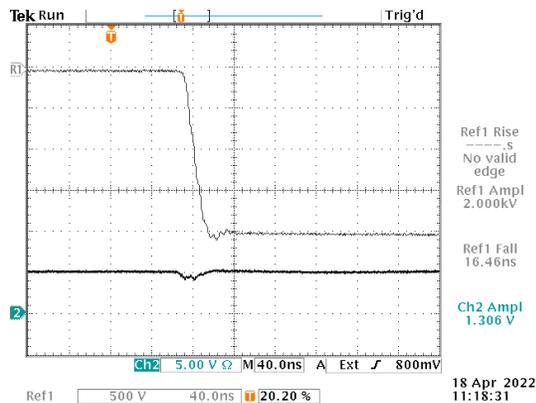
Positive positioning of daughterboard

## TYPICAL NEGATIVE RESULTS (-XHV UNITS)

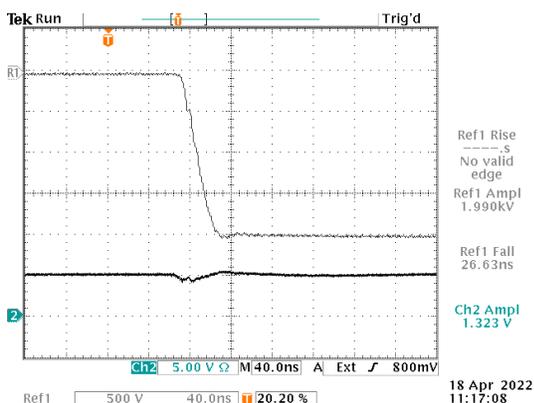
Units with the -XHV option can operate at higher amplitudes, up to 2 kV. The photos below show typical “HV PULSE” waveforms with with AMP1 = -2 kV, and a daughterboard installed in the socketing in the positive position, but with no DUT installed in the DIP8 socket on the daughterboard. (The lower waveform in each photo is the LOGIC OUT “A” output, with R2 = 1 kΩ. A small signal is coupled through parasitic inductance/capacitance in the socketing.)



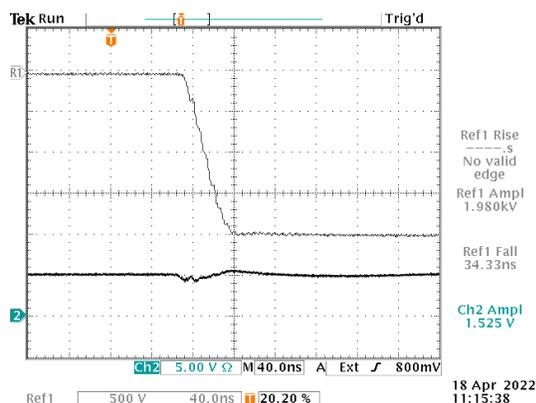
$C = 0 \text{ pF}$ ,  $t_{R10-90} = 6.089 \text{ ns}$



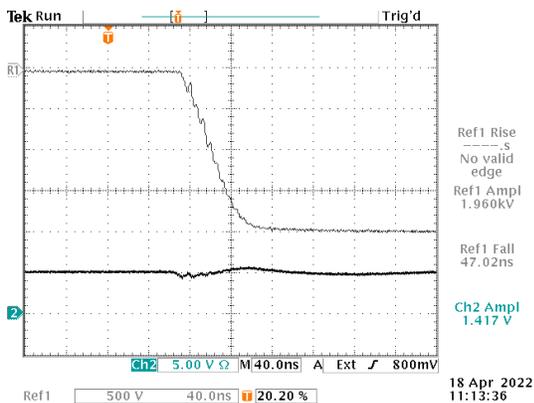
$C = 150 \text{ pF}$ ,  $t_{R10-90} = 16.46 \text{ ns}$



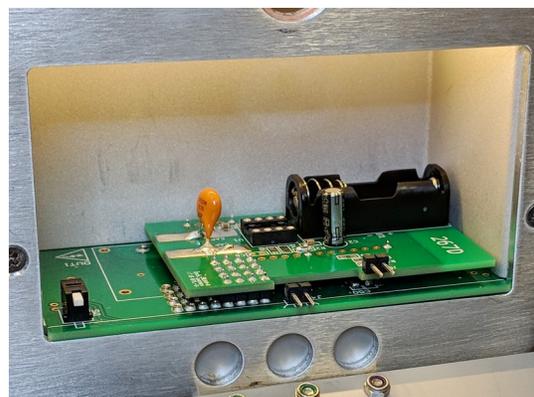
$C = 300 \text{ pF}$ ,  $t_{R10-90} = 26.63 \text{ ns}$



$C = 450 \text{ pF}$ ,  $t_{R10-90} = 34.33 \text{ ns}$



$C = 820 \text{ pF}$ ,  $t_{R10-90} = 47.02 \text{ ns}$



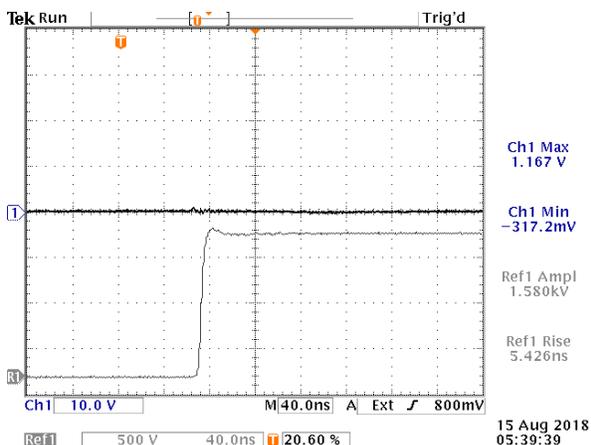
Negative positioning of daughterboard

## VO3120 RESULTS

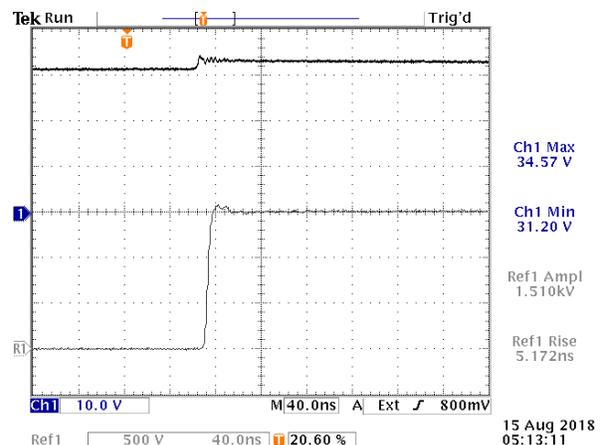
A Vishay VO3120 was tested using  $VCC2 = +32V$ , and the following daughterboard configuration:

Reference	Value	Typical Function
C6	Not used	Load capacitance
R1	Not used	Zero-Ohm Jumper to connect DUT pin 1 to VCC1
R2	Not used	Output pullup
R3	348 $\Omega$ for 10 mA tests, not used for 0 mA tests.	Resistance to connect DUT pin 2 to VCC1. Non-zero resistance for current-drive inputs.
R4	0 $\Omega$	Zero-Ohm Jumper for DUT pin 7 as logic output
R5	Not used	Resistance to connect DUT pin 3 to VCC1
R6	0 $\Omega$	Zero-Ohm Jumper for DUT pin 6 as logic output
R7	Not used	Resistance to connect DUT pin 4 to VCC1
R8	0 $\Omega$	Zero-Ohm Jumper to connect DUT pin 1 to GND1
R9	Not used for 10 mA tests, 0 $\Omega$ for 0 mA tests.	Zero-Ohm Jumper to connect DUT pin 2 to GND1
R10	0 $\Omega$	Zero-Ohm Jumper to connect DUT pin 3 to GND1
R11	0 $\Omega$	Zero-Ohm Jumper to connect DUT pin 4 to GND1
P1, P2	Not used	No rise-time capacitance added between the CAP pads
BT1	One A23-type 12V battery for 10 mA tests, not used for 0 mA tests.	One user-installed A23-type 12V battery, prime power for VCC1. (Please note that A23 batteries have a limited mA·hr rating – typically 30 mA·hr when operating at 15 mA – so the battery should be removed immediately after testing, and its output should be verified to be between 6V and 12V before each test.)

With the daughterboard installed in the socketing in the positive position, and AMP1 set to +1.5 kV and AMP2 set to +32V, these waveforms were obtained:

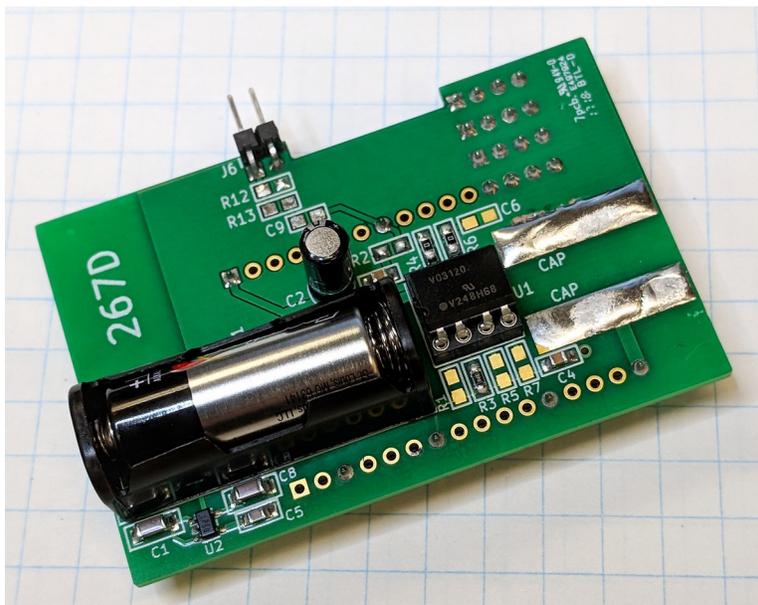


No significant logic output glitch for  $t_{R10-90} = 5.426$  ns, so the CMTI exceeds  $1.5$  kV  $\times$   $(90\%-10\%) / 5.426$  ns = 221 kV/us when  $I_F = 0$  mA.

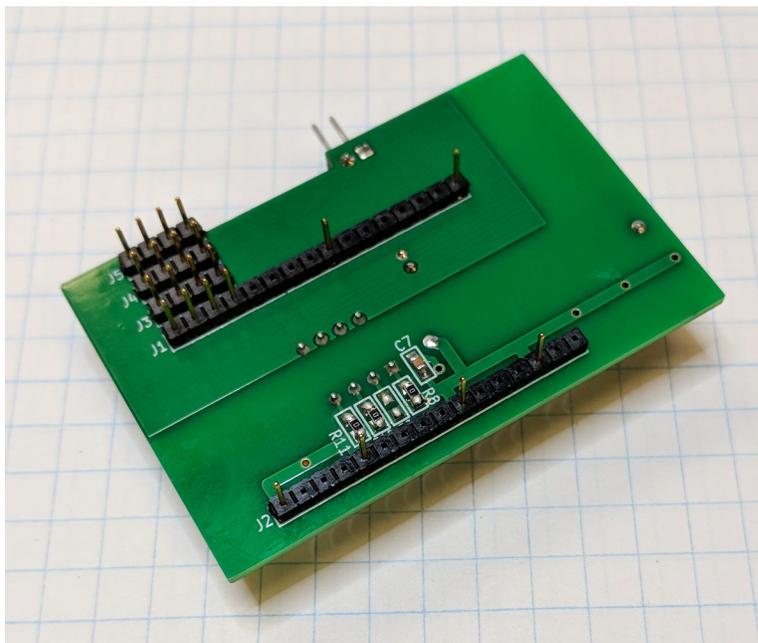


No significant logic output glitch for  $t_{R10-90} = 5.172$  ns, so the CMTI exceeds  $1.5$  kV  $\times$   $(90\%-10\%) / 5.172$  ns = 232 kV/us when  $I_F = 10$  mA.

The actual daughterboard and DUT are shown below, configured for 10 mA of input bias current (with  $R3 = 348$  Ohms and the A23 battery installed):

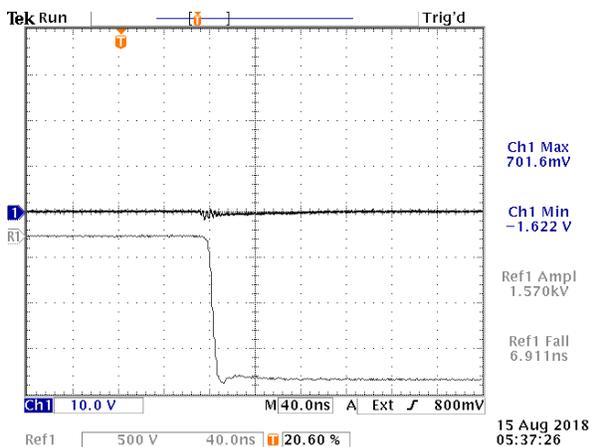


Top side

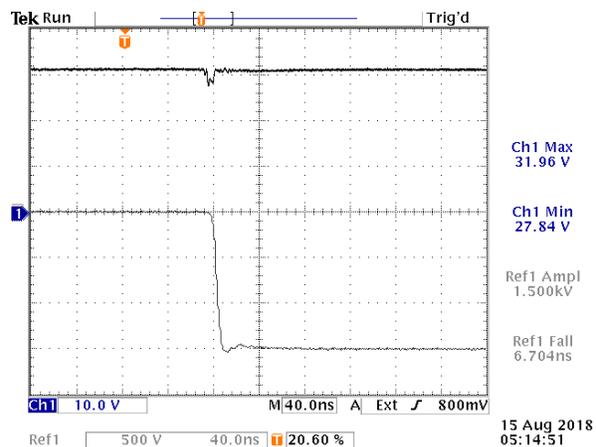


Bottom side

With the daughterboard installed in the socketing in the negative position, and AMP1 set to  $-1.5$  kV and AMP2 set to  $+32$ V, these waveforms were obtained:



No significant logic output glitch for  $t_{R10-90}$   
 $= 6.911$  ns, so the CMTI exceeds  $1.5$  kV  
 $\times (90\%-10\%) / 6.911$  ns =  $174$  kV/us  
 when  $I_F = 0$  mA.



No significant logic output glitch for  $t_{R10-90}$   
 $= 6.704$  ns, so the CMTI exceeds  $1.5$  kV  
 $\times (90\%-10\%) / 6.704$  ns =  $179$  kV/us  
 when  $I_F = 10$  mA.

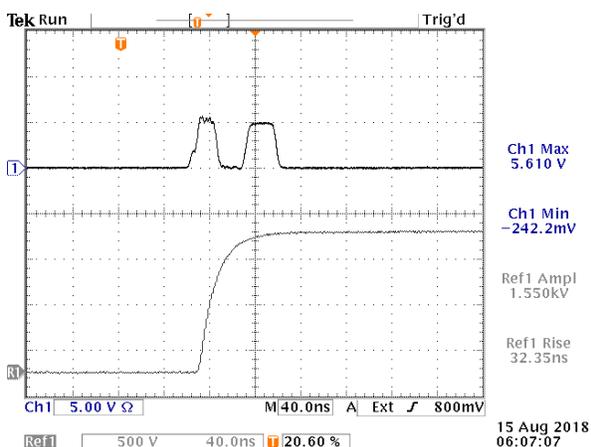
These results show that the VO3120 has very high CMTI tolerance.

## HCPL-7721 RESULTS

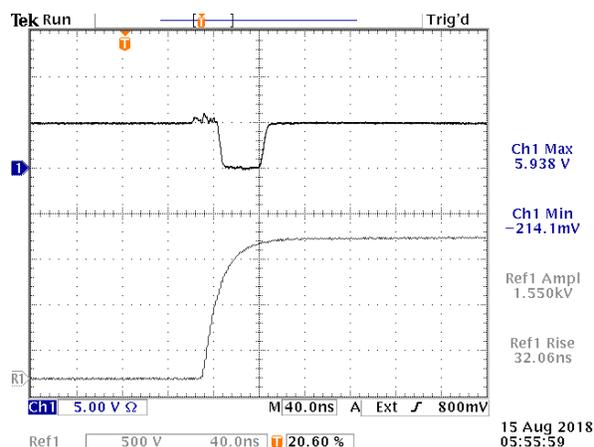
The HP / Agilent / Avago HCPL-7721 is a slower, older device. It was tested using VCC2 = +5V, and the following daughterboard configuration (including a rise time degradation capacitance):

Reference	Value	Typical Function
C6	Not used	Load capacitance
R1	0 $\Omega$	Zero-Ohm Jumper to connect DUT pin 1 to VCC1
R2	Not used	Output pullup
R3	0 $\Omega$ for +5V input tests, not used for 0V input tests.	Resistance to connect DUT pin 2 to VCC1. Non-zero resistance for current-drive inputs.
R4	Not used	Zero-Ohm Jumper for DUT pin 7 as logic output
R5	Not used	Resistance to connect DUT pin 3 to VCC1
R6	0 $\Omega$	Zero-Ohm Jumper for DUT pin 6 as logic output
R7	Not used	Resistance to connect DUT pin 4 to VCC1
R8	Not used	Zero-Ohm Jumper to connect DUT pin 1 to GND1
R9	Not used for +5V input tests, 0 $\Omega$ for 0V input tests.	Zero-Ohm Jumper to connect DUT pin 2 to GND1
R10	Not used	Zero-Ohm Jumper to connect DUT pin 3 to GND1
R11	0 $\Omega$	Zero-Ohm Jumper to connect DUT pin 4 to GND1
P1, P2	150 pF	No rise-time capacitance added between the CAP pads
BT1	One A23-type 12V battery	One user-installed A23-type 12V battery, prime power for VCC1. (Please note that A23 batteries have a limited mA·hr rating – typically 30 mA·hr when operating at 15 mA – so the battery should be removed immediately after testing, and its output should verified to be between 6V and 12V before each test.)

With the daughterboard installed in the socketing in the positive position, and AMP1 set to +1.5 kV and AMP2 set to +5V, these waveforms were obtained:

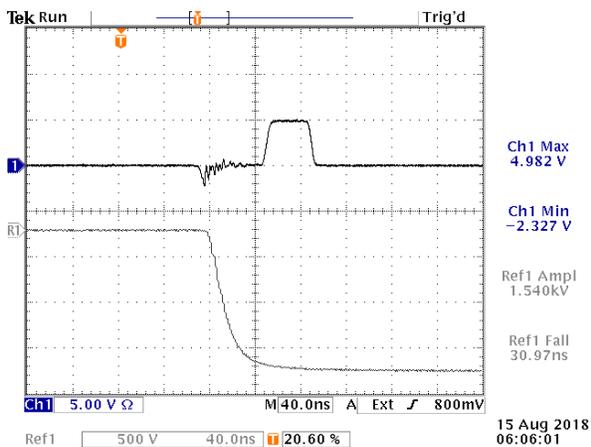


Top = Logic output for 0V input  
Bottom = high voltage pulse

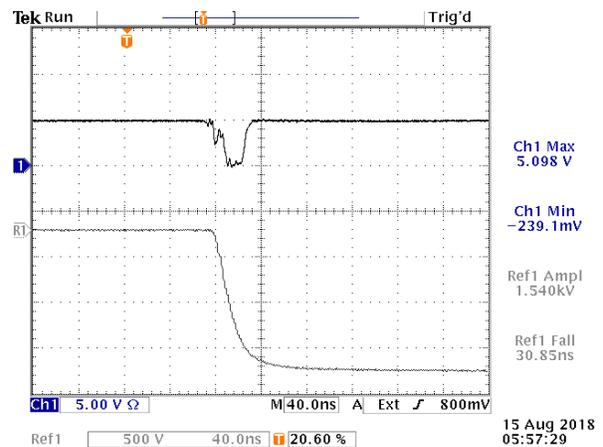


Top = Logic output for 5V input  
Bottom = high voltage pulse

With the daughterboard installed in the socketing in the negative position, and AMP1 set to -1.5 kV and AMP2 set to +5V, these waveforms were obtained:



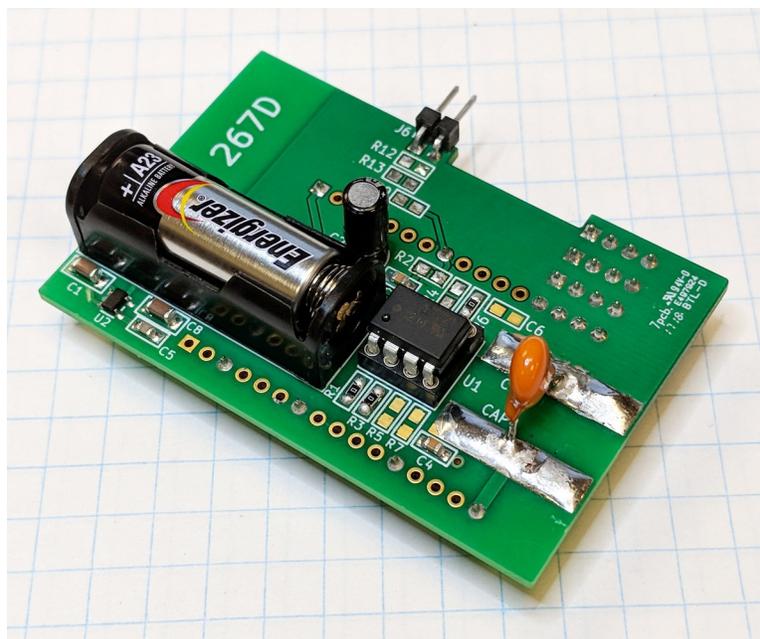
Top = Logic output for 0V input  
Bottom = high voltage pulse



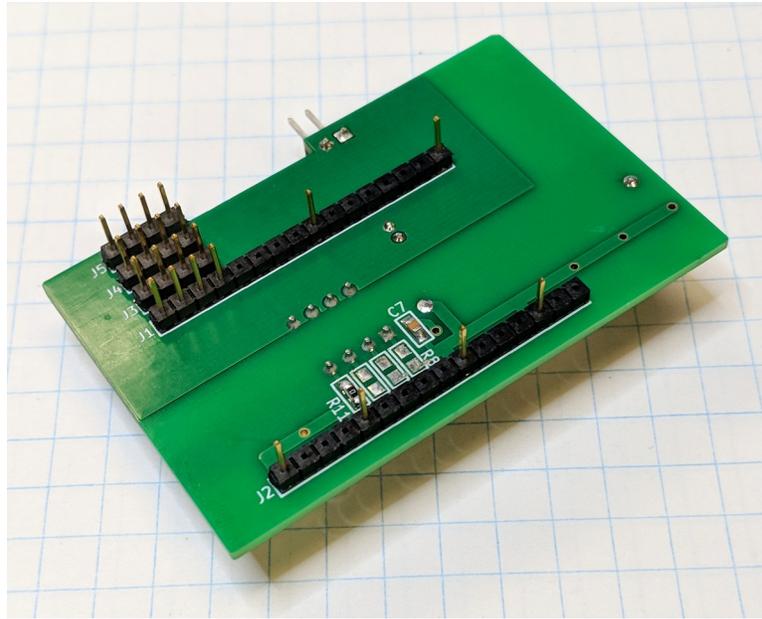
Top = Logic output for 5V input  
Bottom = high voltage pulse

These results show that the HCPL-7721 has a much lower CMTI tolerance than the VO3120.

The actual daughterboard and DUT are shown below, configured for a 5V logic input:



Top side



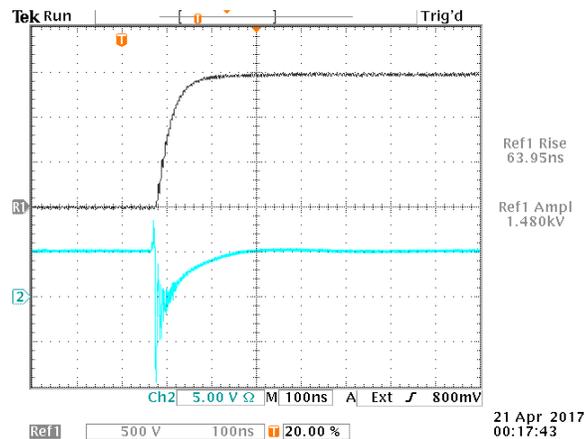
Bottom side

## INDUCTIVE SPIKES AND PROBE SATURATION

Some care must be taken if using a differential probe to sense the logic output. While a differential probe can be useful in reducing the possibility of interference from the high-voltage pulse, it may have strict voltage limits. For example, the Tektronix P6246 is only suitable for values of  $V_{CC2}$  up to +7V. A non-differential probe may be more suitable if  $V_{CC2} > 7V$ .

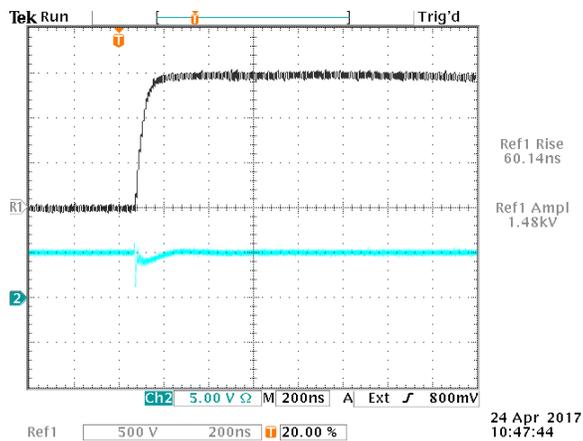
A less obvious problem arises if parasitic inductances or capacitances in the test circuit cause differential voltage spikes exceeding  $\pm 7V$ . The P6246 can saturate heavily under those conditions, which can generate apparent glitch-like transients that are not due to the DUT. Some experimentation may be required by the user in order to identify the best probing arrangement.

Early versions of the AVRQ-5-B were provided with sample daughterboards P/N 267C or earlier. (The current version is 267D). The earlier daughterboards used one or four pins to connect GND2 to the main board socket (which was a ZIF socket). The inductance in the socket pin(s) was sufficient to generate a short voltage spike that could, under some circumstances, overload the P6246 probe. For example, with a 267B daughterboard, a 1k pullup resistor (R2),  $V_{CC} = +5V$ , 300 pF between P1 and P2, and no DUT, the following waveforms were obtained:



This shows an apparent 200 ns wide “glitch” on the logic output. In fact, the P6246 is saturating from the sharp initial inductive voltage spikes, and is taking 200 ns to recover.

To fix this issue, later daughterboards (267C and later) use additional pins to connect GND2 to the main board ZIF socket. This reduces the initial inductive voltage spikes, and prevents probe saturation:



If you are experiencing “unexpected” transients, keep in mind this possibility of probe saturation.

The current version of the AVRQ-5-B no longer uses ZIF socketing, to reduce parasitic inductance further.

Users of AVRQ-5-B models with serial numbers below 13700 may wish to contact Avtech to upgrade their existing unit.

## DC CORRECTNESS ISSUES

The sample daughterboards provided with the AVRQ-5-B are designed to bias the input side of the optocoupler with a fixed bias during the test. To change it, components must be physically changed. This can be problematic with certain devices that do not necessarily power-up to a well-defined state. The NVE IL710 is an example of such a device – as the IL710 datasheet says:

*“To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.”*

The user may wish to add power-up toggle circuitry, or an oscillator, in order to correctly initialize and drive such devices.



## VERIFICATION AND TROUBLESHOOTING

It is sometimes unclear whether the glitches observed on the opto-coupler output are due to the opto-coupler or the test circuit.

To reduce the number of sources of possible interference or error, a daughterboard scheme is used. This allows the drive conditions and the loading to be defined by simple, compact circuits that are user-visible and user-changeable.

Similarly, the floating-side power or bias is derived from a simple battery circuit, whose schematic is included in the schematics section of this manual. A more exotic switching non-battery-based power supply design has been avoided, to minimize complexity. The battery circuit is always active when a battery is installed, allowing current biases to be measured while the DUT is installed in the daughterboard, but the daughterboard is outside of the mainframe. For example, for current-drive devices with non-zero bias levels, the current can typically be measured using compact DMM probes across resistor R3.

 Please note that A23 batteries have a limited mA·hr rating – typically 30 mA·hr when operating at 15 mA – so the battery should be removed immediately after testing, and its output should be verified to be between 6V and 12V before each test.

The high-voltage circuits are only on when the instrument is powered on AND the DUT door is closed AND the output has been set to the “on” state.

 It is NOT possible to measure the drive current or voltage on the floating input side while the high voltage pulse is active. It is dangerous, and it does not work anyway.

 High-voltage differential probes DO NOT accurately reproduce signals if an extremely fast high-voltage common mode signal is present. In other words, their CMTI is worse than that of typical opto-couplers.

 Using two probes and performing oscilloscope-based mathematics to calculate a difference is NOT accurate enough to measure a ~1V differential signal in the presence of a ~ 1.5 kV common mode signal.

If there is doubt about the stability of a non-zero drive signal, try soldering large capacitances across the drive pins of the input to see if that stabilizes anything (taking care to keep the capacitances away from the non-floating circuitry, for safety and interference reasons). If there is no change, that would tend to eliminate the drive signal as a source of problems.

If there is doubt about the stability of a zero-level drive signal, try soldering together the two drive pins directly on the IC package (i.e., short them out), to see if that stabilizes

anything. If there is no change, that would tend to eliminate the drive signal as a source of problems.

Some devices are simply very sensitive to ANY stray capacitance between the input and output sides. Some devices are extremely sensitive to interference coupled to pin 7, which (unwisely) provides a connection to the photo-transistor base. To test this as a possible problem source, try snipping off pin 7 on your device and see if that affects the results beneficially. If it does, you might want to consider designing your own ultra-low-stray-capacitance socket and daughterboard, or avoiding sockets entirely and using soldered devices instead.

## SAFETY CONCERNS

### TURN OUTPUT OFF BEFORE ACCESSING DUT

Always turn the output off before opening the rear-panel DUT door, using the front panel menu or by computer command (“output off”).

If you do not disable the output first, the output will be automatically disabled by a sensor on the DUT door when it is opened. However, the user should not rely on this for safety purposes.

Always check that the front panel indicates that the output is “off” before touching the DUT area.

For maximum safety, turn off the instrument before accessing the DUT area. Ensure that the instrument has been turned off for at least 60 seconds before turning it back on, to allow the embedded controller to reset properly.

### AUTOMATIC TIMEOUT

The output is disabled automatically after 90 seconds of inactivity. The timer resets each time a pulse parameter (amplitude, PRF, etc) is changed.

### OVERLOAD INDICATOR

The front-panel “overload” indicator should always glow green, and never amber (except briefly when the instrument is first turned on).

If the overload indicator becomes active (amber), stop using the instrument immediately.



## OPERATIONAL CHECK

This section describes a sequence to confirm the basic operation of the instrument. It should be performed after receiving the instrument. It is a useful learning exercise as well.

Before proceeding with this procedure, finish reading this instruction manual thoroughly. Then read the “Local Control” section of the “Programming Manual for -B Instruments” thoroughly. The “Local Control” section describes the front panel controls used in this operational check - in particular, the MOVE, CHANGE, and ADJUST controls.

1. With the power off, connect the pulser and the oscilloscope as described in the “Basic Test Arrangement” section on page 53. Install a daughterboard (with no DUT) in the socketing in the positive position.

 Confirm that the scope probe, test load, cables, and any adapters used are rated for 2 kV pulsed operation.

2. Turn on the AVRQ-5-B. The main menu will appear on the LCD.
3. To set the AVRQ-5-B to trigger from the internal clock at a PRF of 10 Hz:
  - a) The arrow pointer should be pointing at the frequency menu item. If it is not, press the MOVE button until it is.
  - b) Press the CHANGE button. The frequency submenu will appear. Rotate the ADJUST knob until the frequency is set at 10 Hz.
  - c) The arrow pointer should be pointing at the “Internal” choice. If it is not, press MOVE until it is.
  - d) Press CHANGE to return to the main menu.
4. To set the delay to 50 ns:
  - a) Press the MOVE button until the arrow pointer is pointing at the delay menu item.
  - b) Press the CHANGE button. The delay submenu will appear. Rotate the ADJUST knob until the delay is set at 50 ns.
  - c) The arrow pointer should be pointing at the “Normal” choice. If it is not, press MOVE until it is.
  - d) Press CHANGE to return to the main menu.

5. To set the HV PULSE amplitude to +1.5 kV:
  - a) Press the MOVE button until the arrow pointer is pointing at the AMP1 menu item.
  - b) Press the CHANGE button. The submenu will appear. Rotate the ADJUST knob until the amplitude is set at +1.5 kV.
  - c) Press CHANGE to return to the main menu.
6. To set the VCC2 amplitude to +5V:
  - a) Press the MOVE button until the arrow pointer is pointing at the AMP2 menu item.
  - b) Press the CHANGE button. The submenu will appear. Rotate the ADJUST knob until the amplitude is set at +5V.
  - c) Press CHANGE to return to the main menu.
7. At this point, nothing should appear on the oscilloscope.
8. To enable the output:
  - a) Press the MOVE button until the arrow pointer is pointing at the output menu item.
  - b) Press the CHANGE button. The output submenu will appear.
  - c) Press MOVE until the arrow pointer is pointing at the "ON" choice.
  - d) Observe the oscilloscope. You should see +1.5 kV pulses with < 10 ns rise time, approximately.
  - e) Press CHANGE to return to the main menu.
9. 90 seconds after the last parameter change, the instrument will automatically shut the output off. Confirm that this occurs.

This completes the operational check.

## PROTECTING YOUR INSTRUMENT

### USE HIGH-VOLTAGE CABLES, CONNECTORS, AND PROBES

 Confirm that the scope probe and any adapters used on the HV PULSE output are rated for at least 2 kV pulsed operation.

### SHORT-CIRCUIT PROTECTION

The output will withstand temporary short-circuit conditions. However, short-circuit conditions should not be allowed to persist longer than 10 seconds, or the stress on the components will shorten the circuit lifetime.



## MECHANICAL INFORMATION

### TOP COVER REMOVAL

If necessary, the interior of the instrument may be accessed by removing the four Phillips screws on the top panel. With the four screws removed, the top cover may be slid back (and off).

 Always disconnect the power cord and allow the instrument to sit unpowered for 10 minutes before opening the instrument. This will allow any internal stored charge to discharge.

There are no user-adjustable internal circuits. For repairs other than fuse replacement, please contact Avtech ([info@avtechpulse.com](mailto:info@avtechpulse.com)) to arrange for the instrument to be returned to the factory for repair.

 Caution: High voltages (over 2000V) are present inside the instrument during normal operation. Do not operate the instrument with the cover removed.

 Caution: Do not remove the internal aluminum lid. It shields certain very-high-voltage areas.

### RACK MOUNTING

A rack mounting kit is available. The -R6 rack mount kit may be installed after first removing the one Phillips screw on the side panel adjacent to the front handle.



## MAINTENANCE

### REGULAR MAINTENANCE

This instrument does not require any regular maintenance. Traceable calibration of the pulse parameters should be established using a calibrated measurement of the output, rather than relying on instrument settings.

On occasion, one or more of the four rear-panel fuses may require replacement. All fuses can be accessed from the rear panel. See the “FUSES” section for details.

### CLEANING

If desired, the interior of the instrument may be cleaned using compressed air to dislodge any accumulated dust. (See the “TOP COVER REMOVAL” section for instructions on accessing the interior.) No other cleaning is recommended.

### TRIGGER DAMAGE

The rear-panel TRIG input, used in the external trigger mode, is protected by a diode clamping circuit. However, the protection circuit is not foolproof, and it is possible for a grossly excessive signal to damage the trigger circuitry on the main timing control board (the 4×10 inch board on the right side of the instrument).

The IC that is most likely to fail under these conditions is installed in a socket. It is a standard TTL IC in a 16-pin plastic DIP package, model 74F151 or equivalent.

If you suspect that this IC has been damaged, turn off the power and replace this IC. It may be replaced by a 74F151, 74LS151, 74ALS151, or 74HCT151.



## PROGRAMMING YOUR PULSE GENERATOR

### KEY PROGRAMMING COMMANDS

The “Programming Manual for -B Instruments” describes in detail how to connect the pulse generator to your computer, and the programming commands themselves. A large number of commands are available; however, normally you will only need a few of these. Here is a basic sample sequence of commands that might be sent to the instrument after power-up:

*rst	(resets the instrument)
trigger:source internal	(selects internal triggering)
frequency 10 Hz	(sets the frequency to 10 Hz)
pulse:delay 1 us	(sets the delay to 100 ns)
volt1 +1.5 kV	(sets the HV PULSE amplitude to +1.5 kV)
volt2 5.0	(sets VCC2 to +5.0V)
output on	(turns on the output)

The output will turn off automatically 90 seconds later, if no further commands are sent before then.

For triggering a single event, this sequence would be more appropriate:

*rst	(resets the instrument)
trigger:source hold	(turns off all triggering)
volt1 -1.5 kV	(sets the HV PULSE amplitude to -1.5 kV)
volt2 5.0	(sets VCC2 to +5.0V)
output on	(turns on the output)
trigger:source immediate	(generates a single non-repetitive trigger event)
trigger:source hold	(turns off all triggering)
output off	(turns off the output)

To set the instrument to trigger from an external TTL signal applied to the rear-panel TRIG connector, use:

*rst	(resets the instrument)
trigger:source external	(selects external triggering)
pulse:delay 1 us	(sets the delay to 100 ns)
volt1 -1.5 kV	(sets the HV PULSE amplitude to -1.5 kV)
volt2 5.0	(sets VCC2 to +5.0V)
output on	(turns on the output)

These commands will satisfy 90% of your programming needs.

## ALL PROGRAMMING COMMANDS

For more advanced programmers, a complete list of the available commands is given below. These commands are described in detail in the “Programming Manual for -B Instruments”. (Note: this manual also includes some commands that are not implemented in this instrument. They can be ignored.)

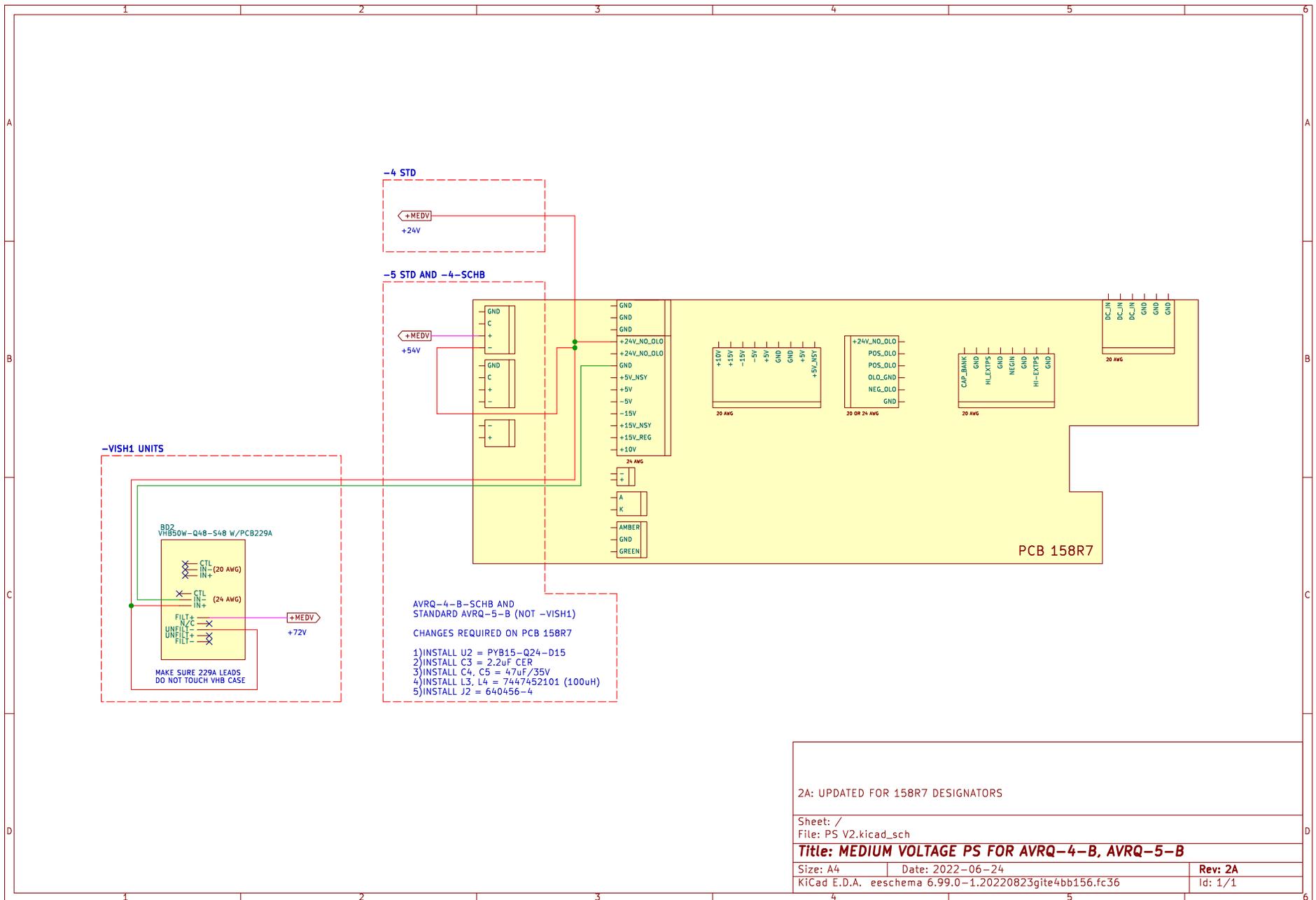
<u>Keyword</u>	<u>Parameter</u>	<u>Notes</u>
OUTPut:		
:[STATe]	<boolean value>	
:PROTection		
:TRIPped?		[query only]
[SOURce]:		
:FREQuency		
[:CW   FIXed]	<numeric value>	
[SOURce]:		
:PULSe		
:PERiod	<numeric value>	
:HOLD	WIDTh   DCYCLE	
:DELay	<numeric value>	
:GATE		
:TYPE	ASYNc   SYNc	
:LEVel	HIGH   LOW	
:VOLTage		
[:LEVel]		
[:IMMediate]		
[:AMPLitude]	<numeric value>   EXTERNAL	
STATUS:		
:OPERation		
:[EVENT]?		[query only, always returns "0"]
:CONDition?		[query only, always returns "0"]
:ENABle	<numeric value>	[implemented but not useful]
:QUEStionable		
:[EVENT]?		[query only, always returns "0"]
:CONDition?		[query only, always returns "0"]
:ENABle	<numeric value>	[implemented but not useful]
SYSTEM:		
:COMMunicate		
:GPIB		
:ADDRes	<numeric value>	
:SERial		
:CONTRol		
:RTS	ON   IBFull   RFR	
:[RECeive]		
:BAUD	1200   2400   4800   9600   19200   38400   57600   115200	
:ERRor		
:[NEXT]?		[query only]
:COUNT?		[query only]
:VERSion?		[query only]
TRIGger:		
:SOURce	INTERNAL   EXTERNAL   MANUAL   HOLD   IMMEDIATE	
*CLS		[no query form]
*ESE	<numeric value>	
*ESR?		[query only]
*IDN?		[query only]

*OPC		
*SAV	0   1   2   3	[no query form]
*RCL	0   1   2   3	[no query form]
*RST		[no query form]
*SRE	<numeric value>	
*STB?		[query only]
*TST?		[query only]
*WAI		[no query form]



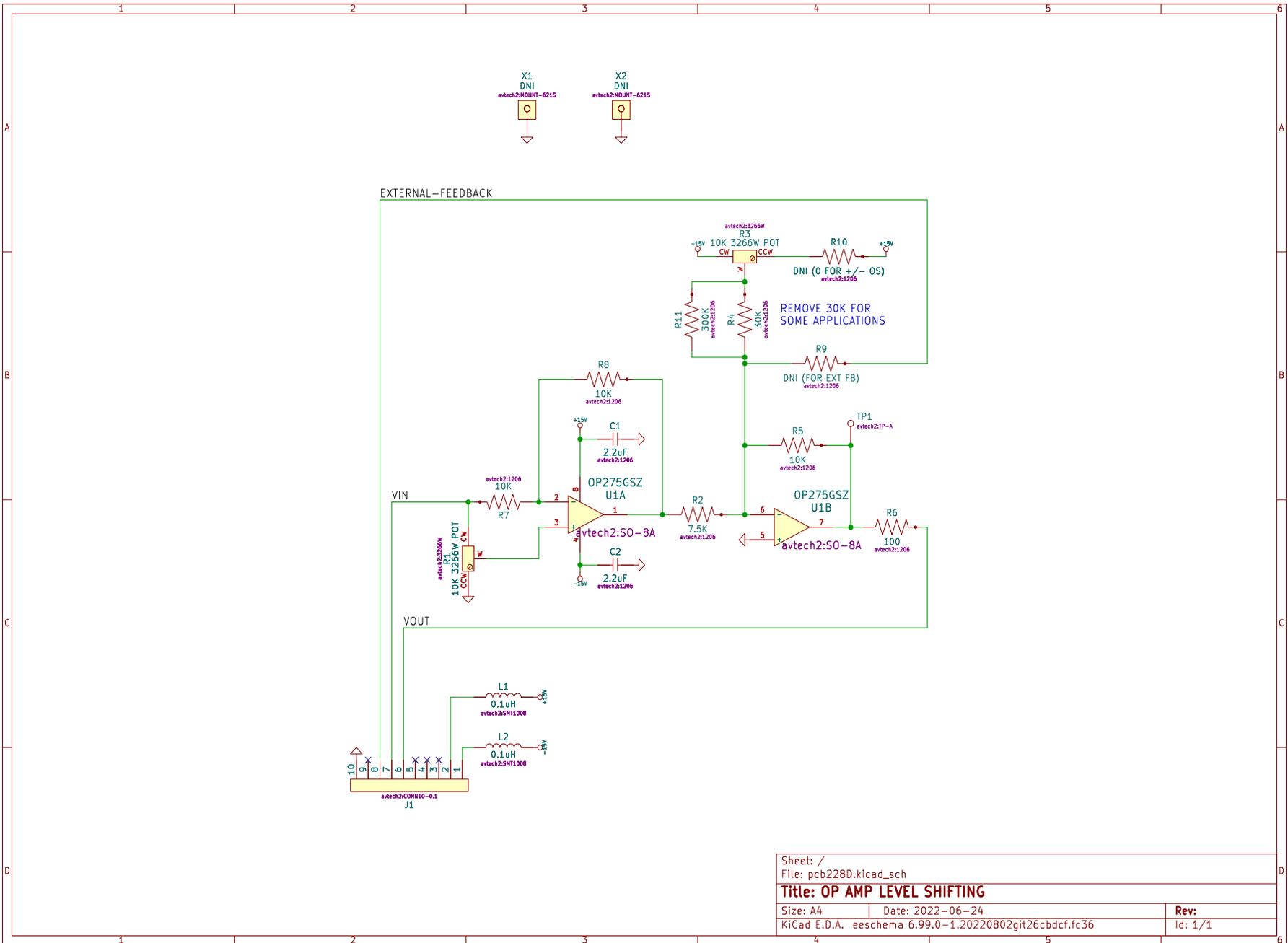


# MEDIUM VOLTAGE POWER SUPPLY



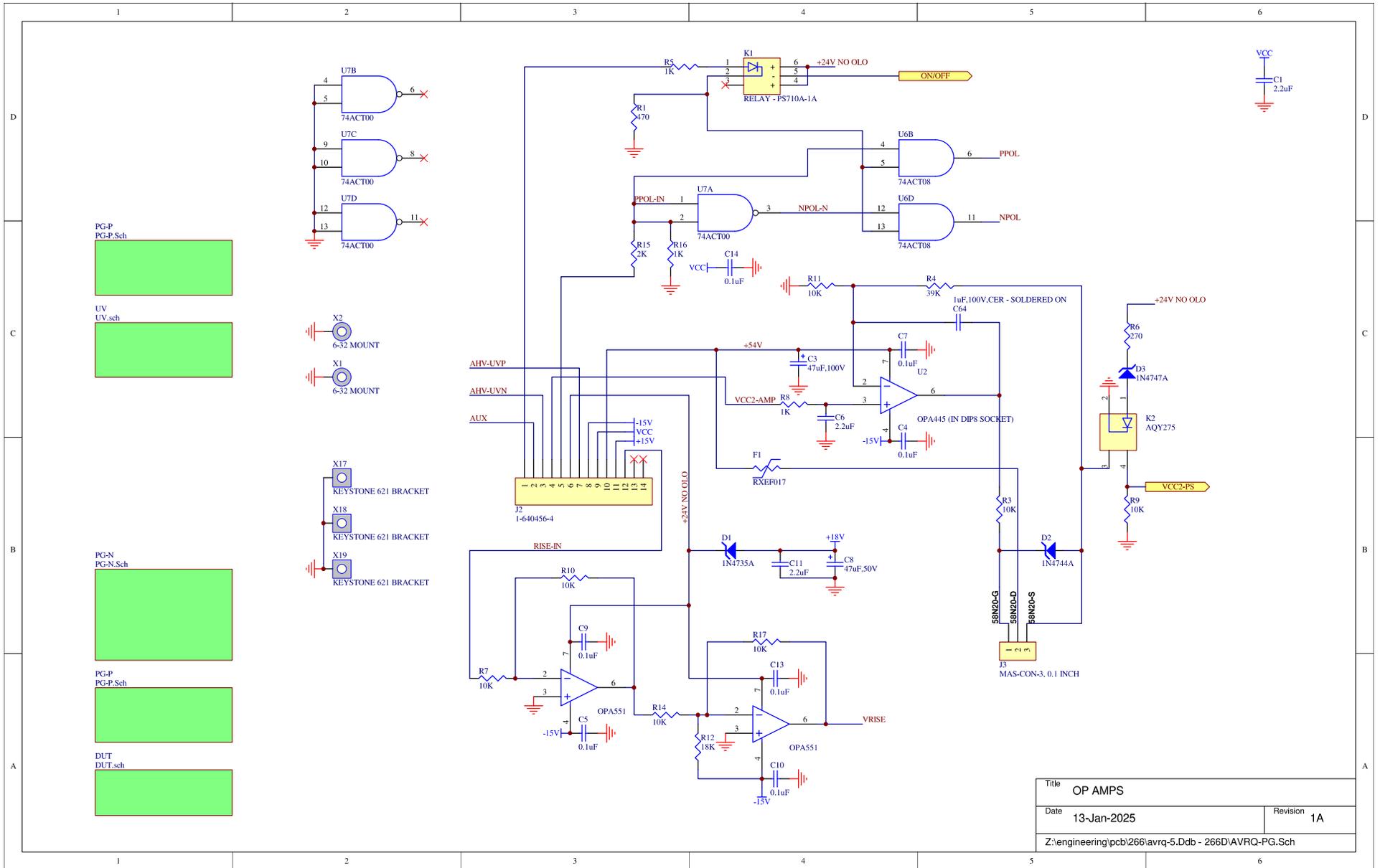


# PCB 228D - OP AMPS (-AHV AND -XHV UNITS)



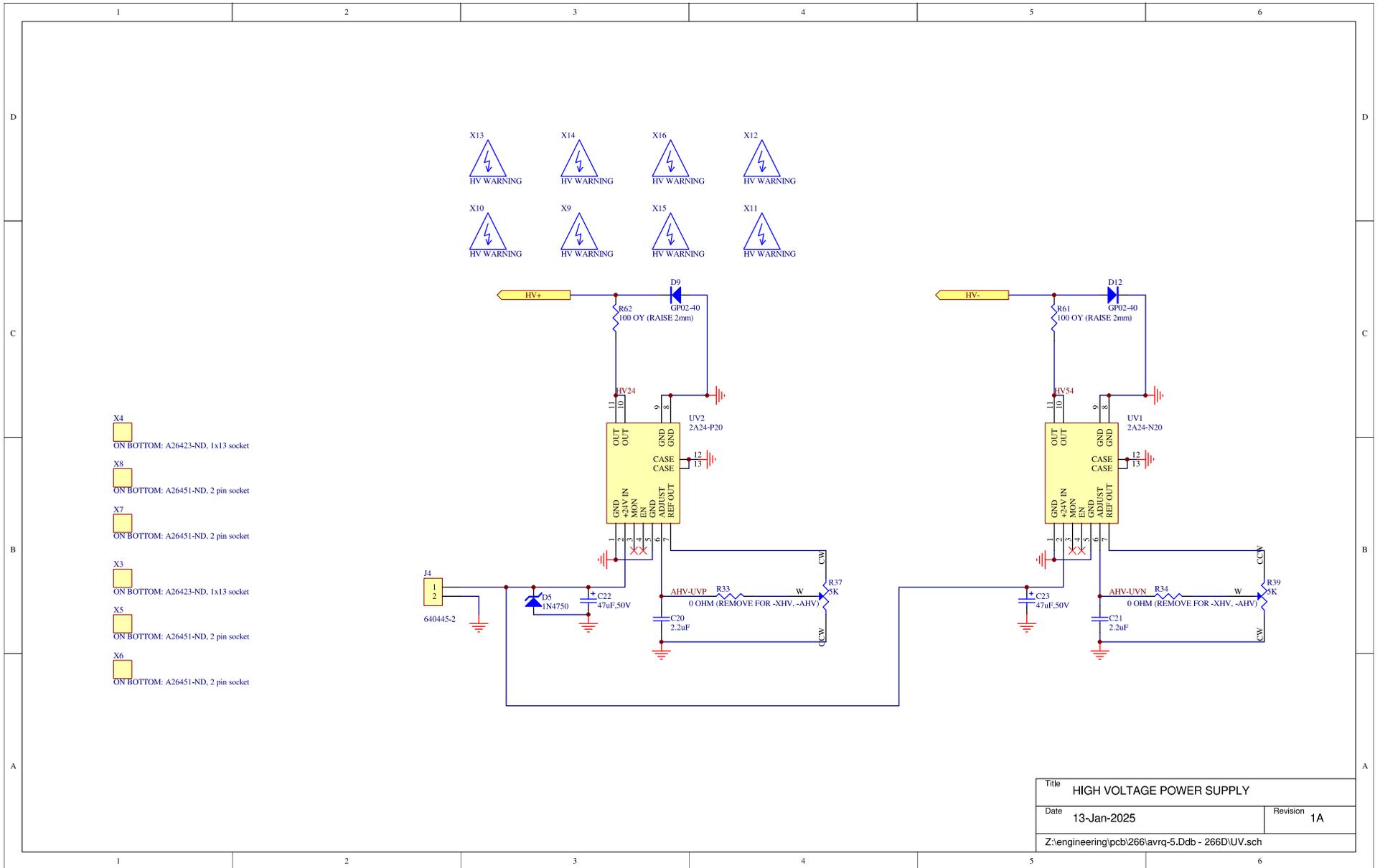
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Size: A4	Date: 2022-06-24	Rev:	
KiCad E.D.A. eeschema 6.99.0-1.20220802git26cbdcf.fc36			Id: 1/1

# PCB 266D - PULSER, 1 OF 6, OP AMPS



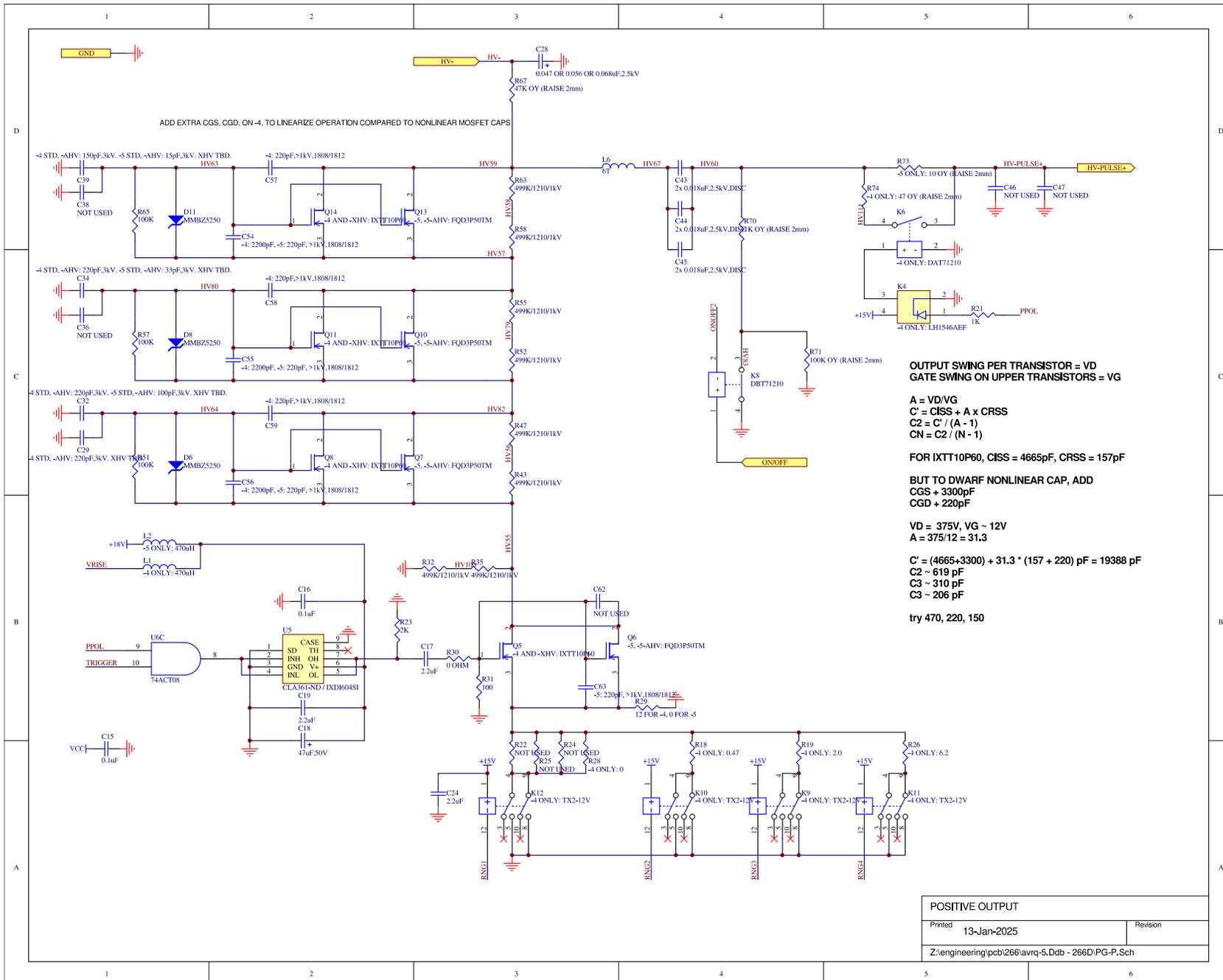
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Date	13-Jan-2025	Revision	1A
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# PCB 266D - PULSER, 2 OF 6, HVPS

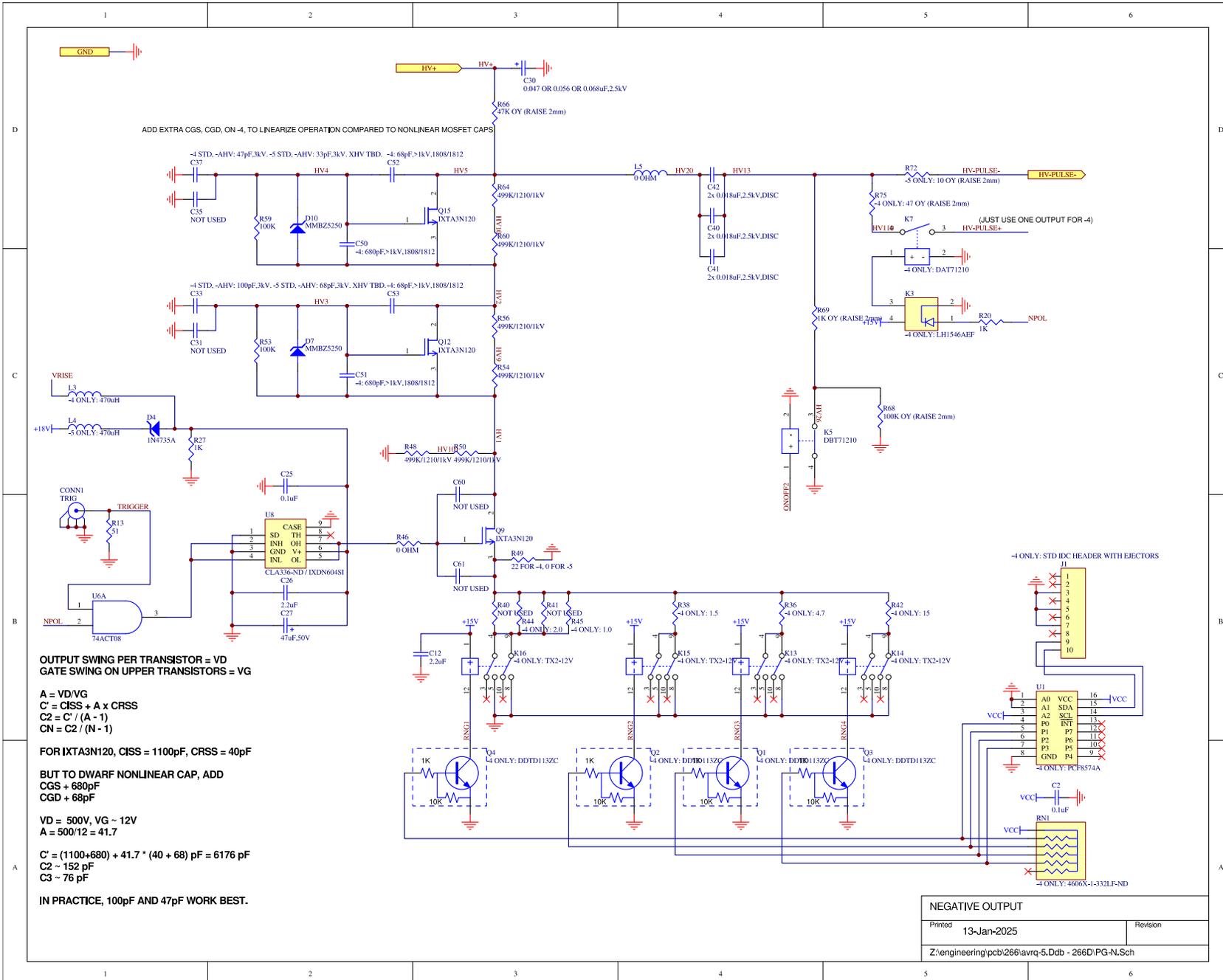


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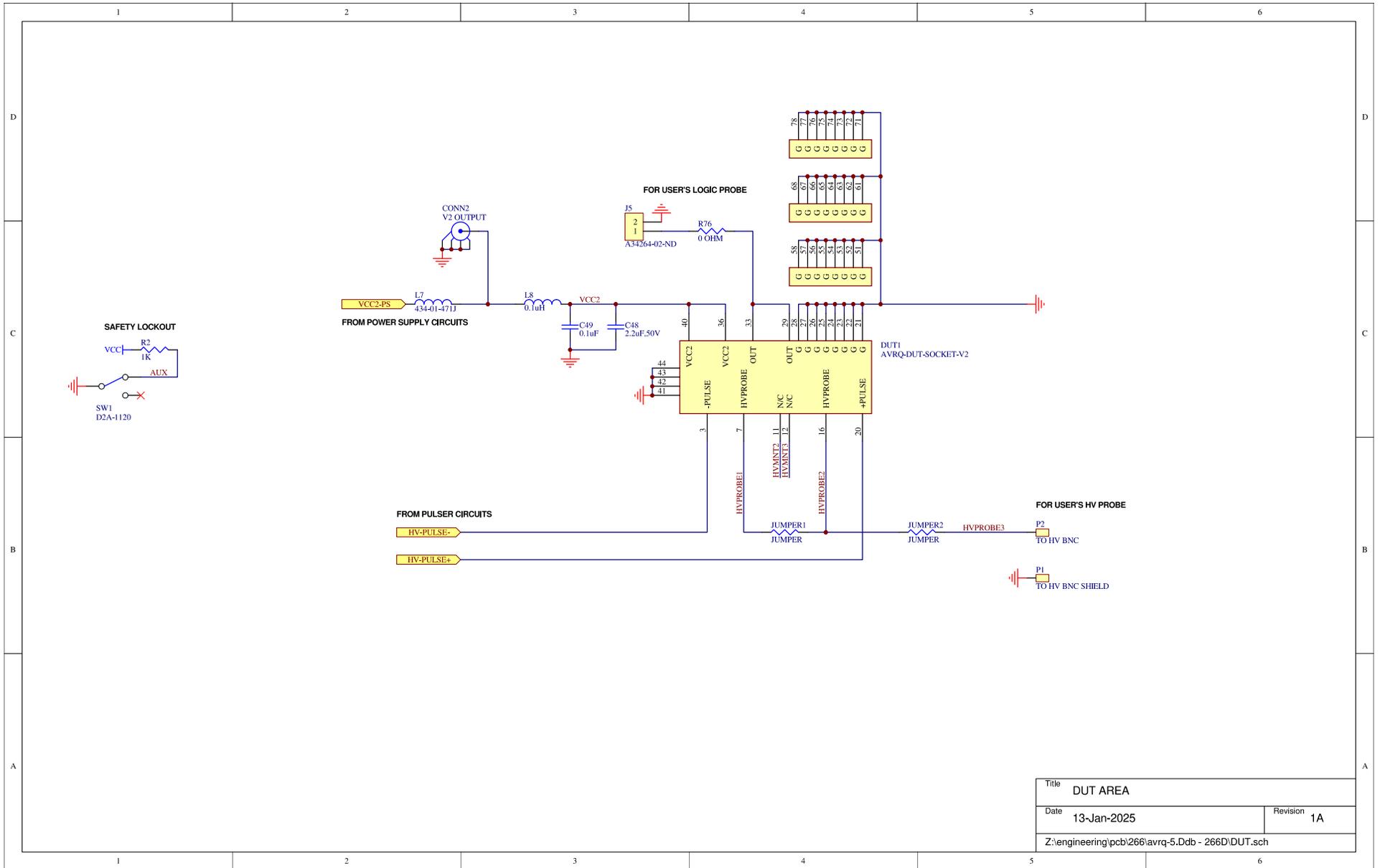
# PCB 266D - PULSER, 3 OF 6, POSITIVE OUTPUT



# PCB 266D - PULSER, 4 OF 6, NEGATIVE OUTPUT



# PCB 266D - PULSER, 5 OF 6, DUT AREA



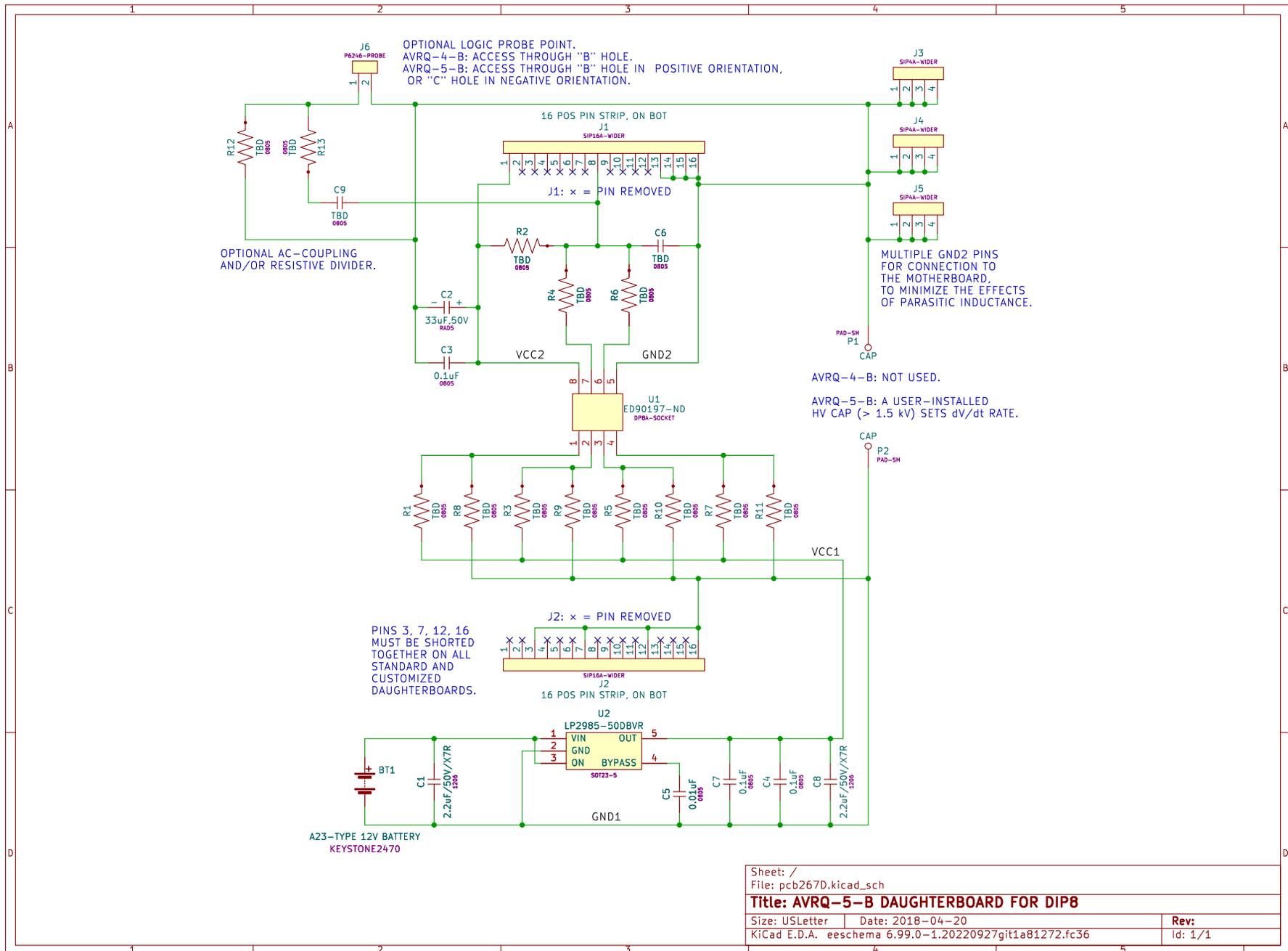
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Date	13-Jan-2025	Revision 1A
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PCB 266D - PULSER, 6 OF 6, COMPONENT CONFIGURATIONS

PCB 266D CONFIGURATIONS FOR DIFFERENT MODELS:

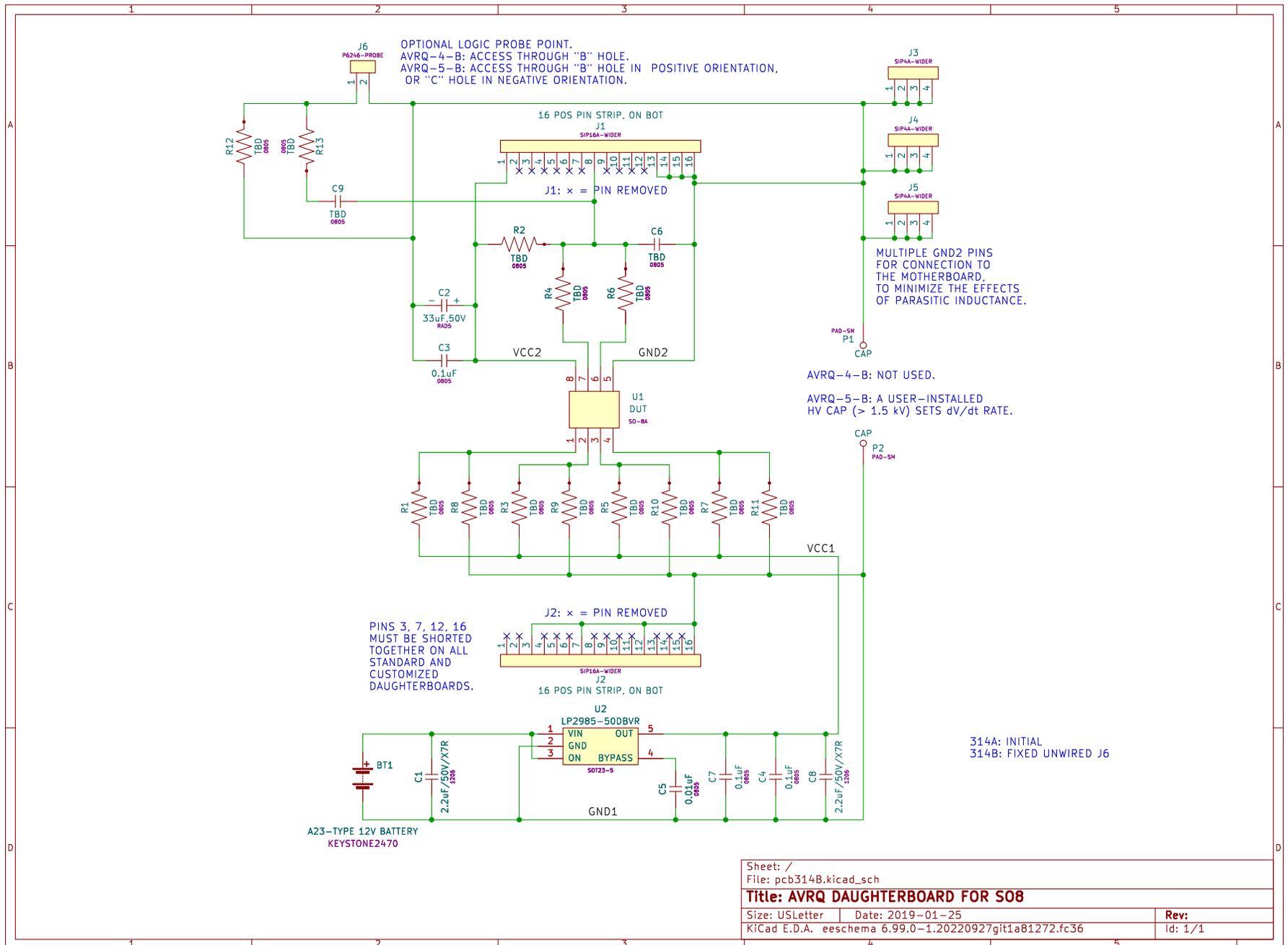
			AVRQ-4	AVRQ-4-AHV	AVRQ-4-XHV	AVRQ-5	AVRQ-5-AHV	AVRQ-5-XHV
□ 3		Q9 Q12 Q15	IXTA3N120 x1					IXTA3N120 x3, stacked
□ 1 □ 1	NEG OUT	C31 C33	100 pF, 3 kV not used		← same	68 pF, 3 kV not used		100 pF, 3 kV 100 pF, 3 kV
□ 1 □ 1		C35 C37	47 pF, 3 kV not used		← same	33 pF, 3 kV not used		100 pF, 3 kV not used
□ 2		C50 C51 (between pins 1+3 of Q, linearizes C <sub>GS</sub> )	680pF, 3kV		← same	Not used		
□ 2		C52 C53 (between pins 1+tab of Q, linearize C <sub>GD</sub> )	68pF, 3kV		← same	Not used		
□ 4		Q5/6 Q7/8 Q10/11 Q13/14	IXTT10P60			FQD3P50TM		IXTT10P60
□ 1 □ 1	POS OUT	C29 C32	220 pF, 3 kV 220 pF, 3 kV		← same	100 pF, 3 kV not used		220 pF, 3 kV 220 pF, 3 kV
□ 1 □ 1		C34 C36	220 pF, 3 kV not used		← same	33 pF, 3 kV not used		220 pF, 3 kV not used
□ 1 □ 1		C38 C39	150 pF, 3 kV not used		← same	15 pF, 3 kV not used		150 pF, 3 kV not used
□ 3		C54 C55 C56 (between pins 1+3 of Q, linearize C <sub>GS</sub> )	2200 pF, 3 kV		← same	220 pF, 3 kV		2200 pF, 3 kV
□ 3		C57 C58 C59 (between pins 1+tab of Q, linearize C <sub>GD</sub> )	220 pF, 3 kV		← same	Not used		47pF, 3kV
• 2		UV	R33 R34	0 OHMS	Not used		0 OHMS	Not used
• 2	ZOUT	R72 R73	Not used			47 OY (RAISE 2mm)		27 OY (RAISE 2mm)
• 2		R74 R75	47 OY (RAISE 2mm)			Not used		
• 2	VDRV	L2 L4	Not used			470 uH		
• 2		L1 L3	470 uH			Not used		
• 1	RMIN	R29	12 OHMS			0 OHMS		
• 1		R49	22 OHMS			0 OHMS		

# DUT WIRING, ON STANDARD DAUGHTERBOARD (PCB 267D)

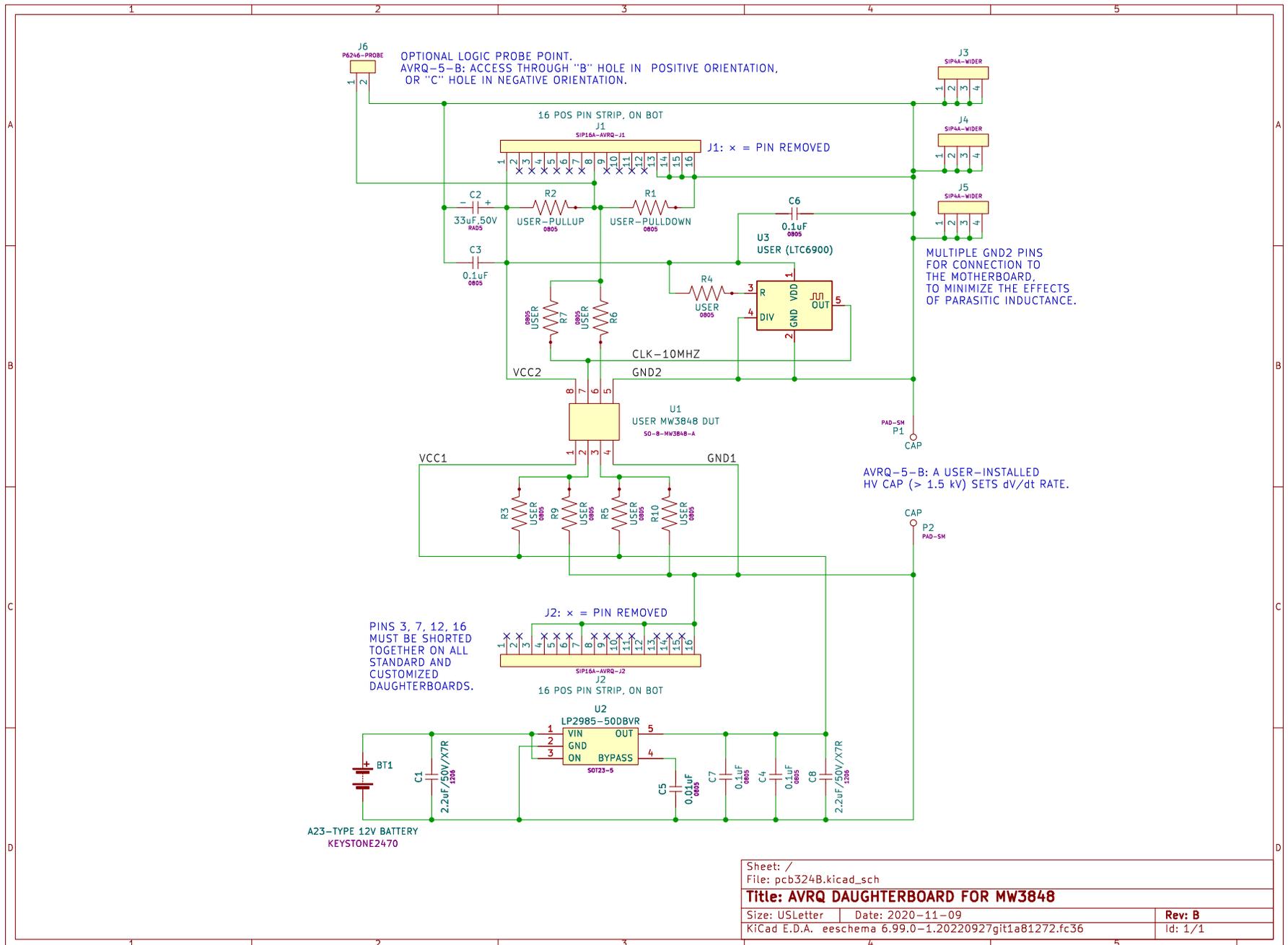


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Size: USLetter	Date: 2018-04-20	Rev:	
KiCad E.D.A. eeschema 6.99.0-1.20220927git1a81272.fc36	Id: 1/1		

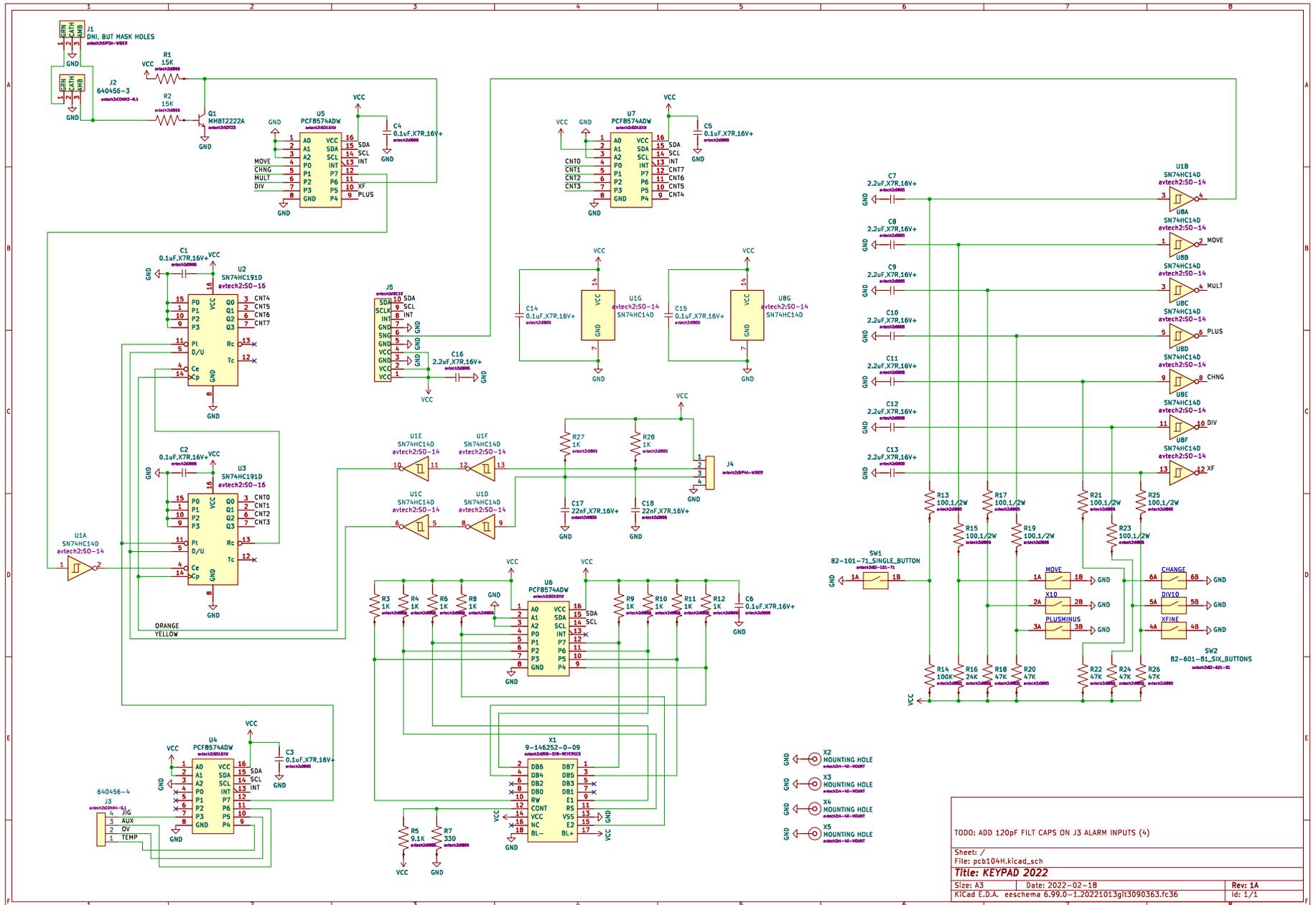
# DUT WIRING, ON S08 DAUGHTERBOARD (PCB 314B)



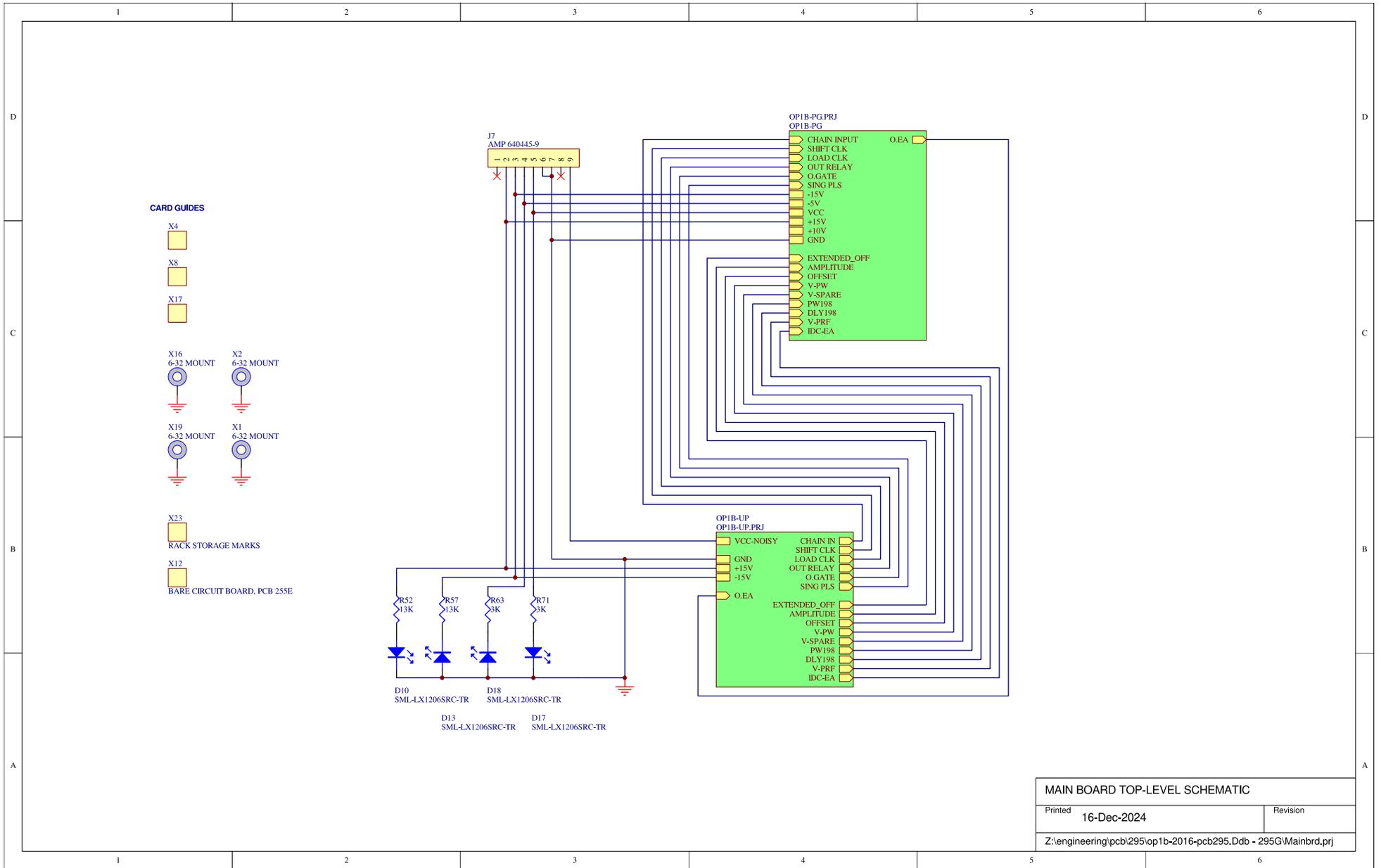
# DUT WIRING, ON CUSTOMER-SPECIFIC DAUGHTERBOARD (PCB 324B)



# PCB 104H - KEYPAD / DISPLAY BOARD

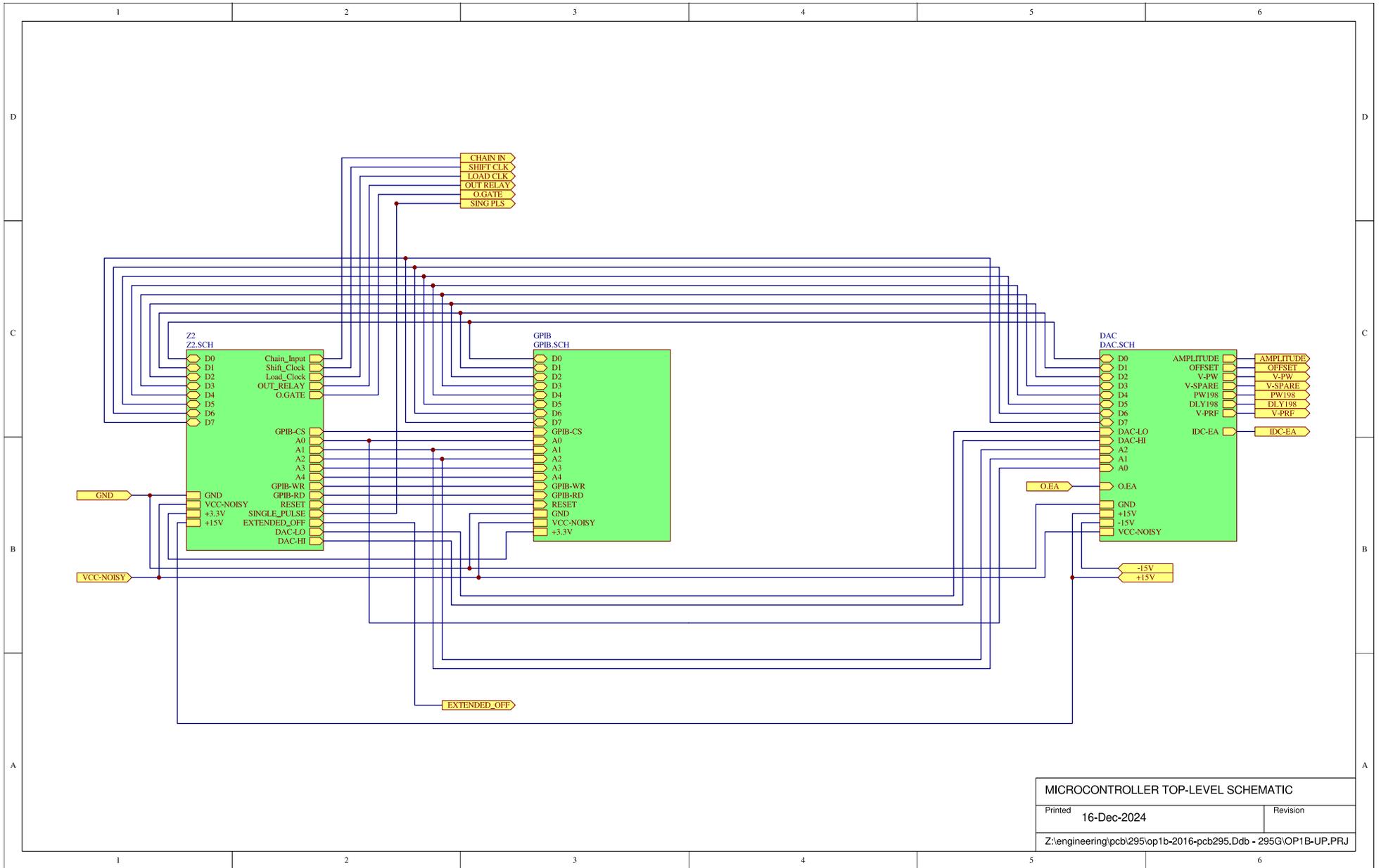


# PCB 295G - MAIN CONTROL BOARD, 1 OF 13, TOP-LEVEL



MAIN BOARD TOP-LEVEL SCHEMATIC	
Printed	Revision
16-Dec-2024	
Z:\engineering\pcb\295\op1b-2016-pcb295.Ddb - 295G>Mainbrd.prj	

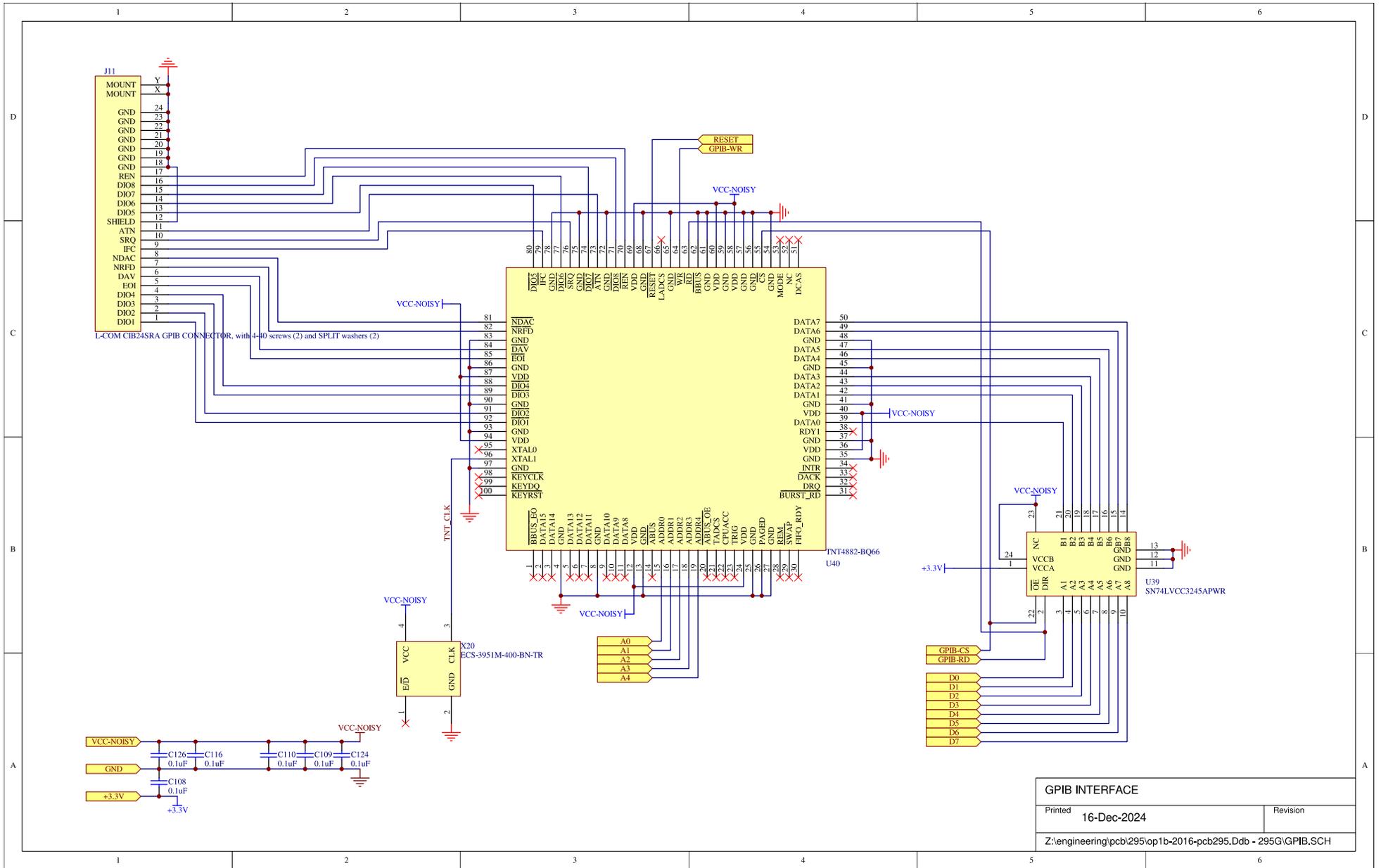
# PCB 295G - MAIN CONTROL BOARD, 2 OF 13, MICROCONTROLLER TOP-LEVEL



MICROCONTROLLER TOP-LEVEL SCHEMATIC	
Printed	16-Dec-2024
Revision	
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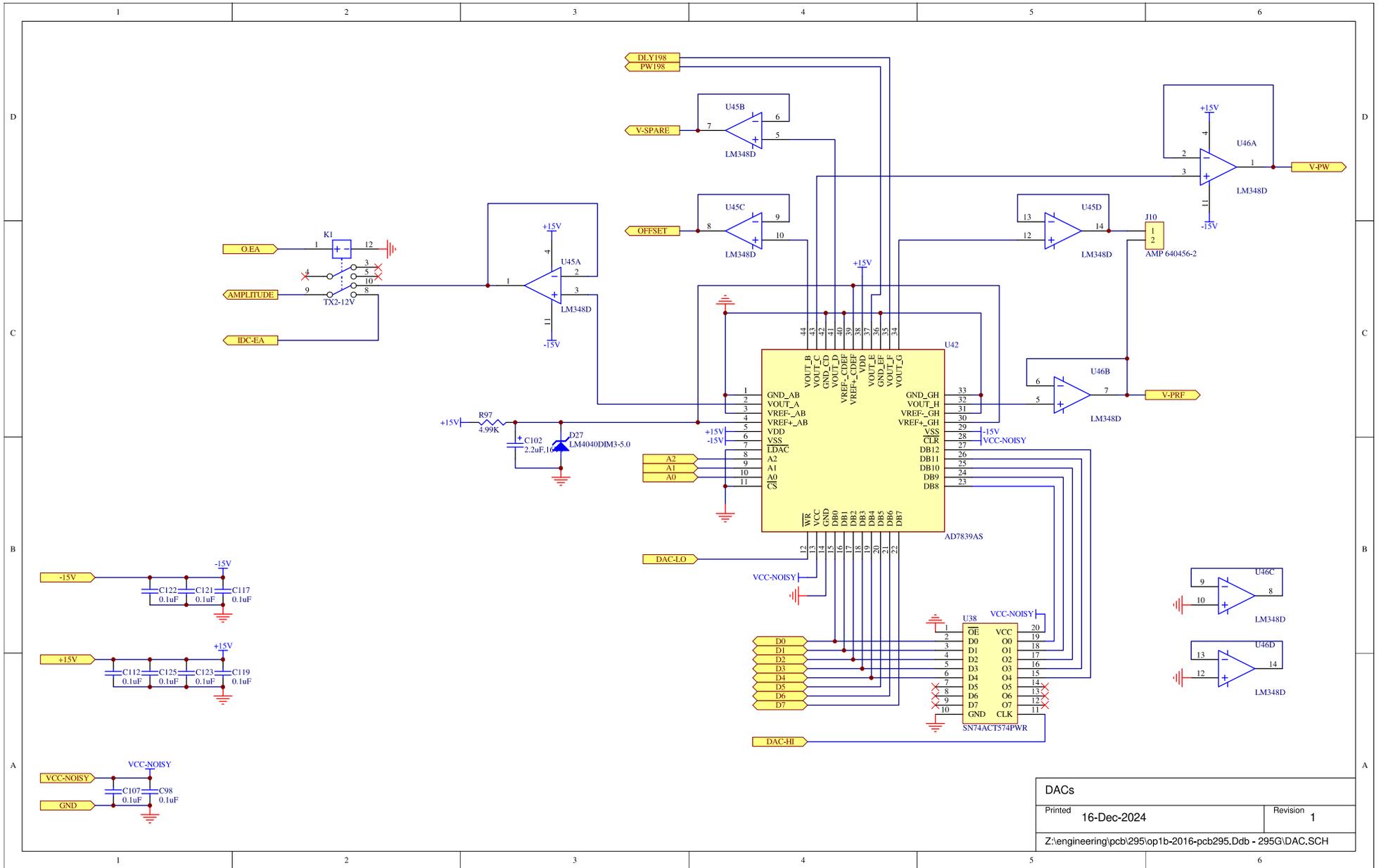


# PCB 295G - MAIN CONTROL BOARD, 4 OF 13, GPIB INTERFACE

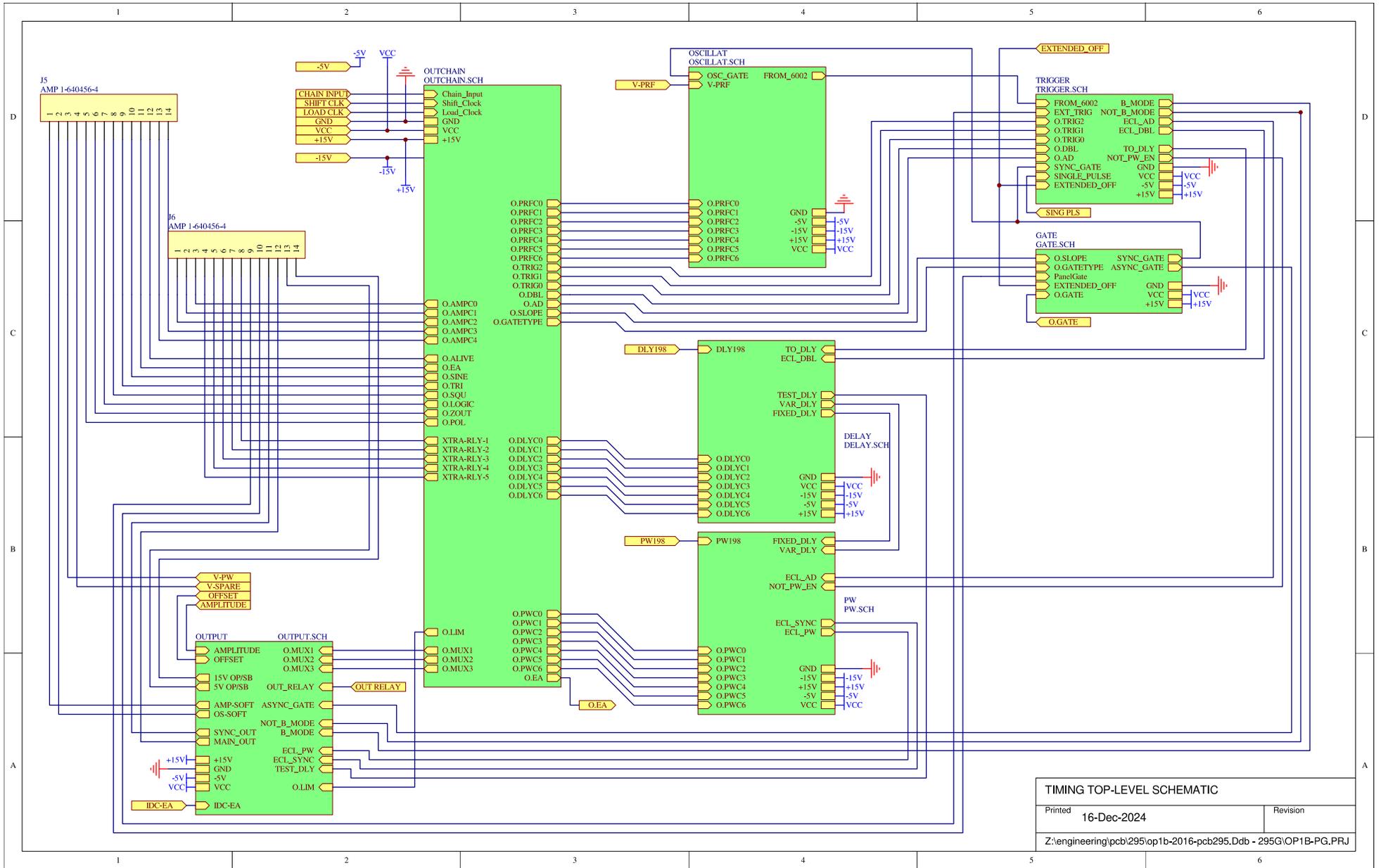


GPIB INTERFACE	
Printed	Revision
16-Dec-2024	
Z:\engineering\pcb\295\op1b-2016-pcb295.Ddb - 295G\GPIB.SCH	

# PCB 295G - MAIN CONTROL BOARD, 5 OF 13, DACs

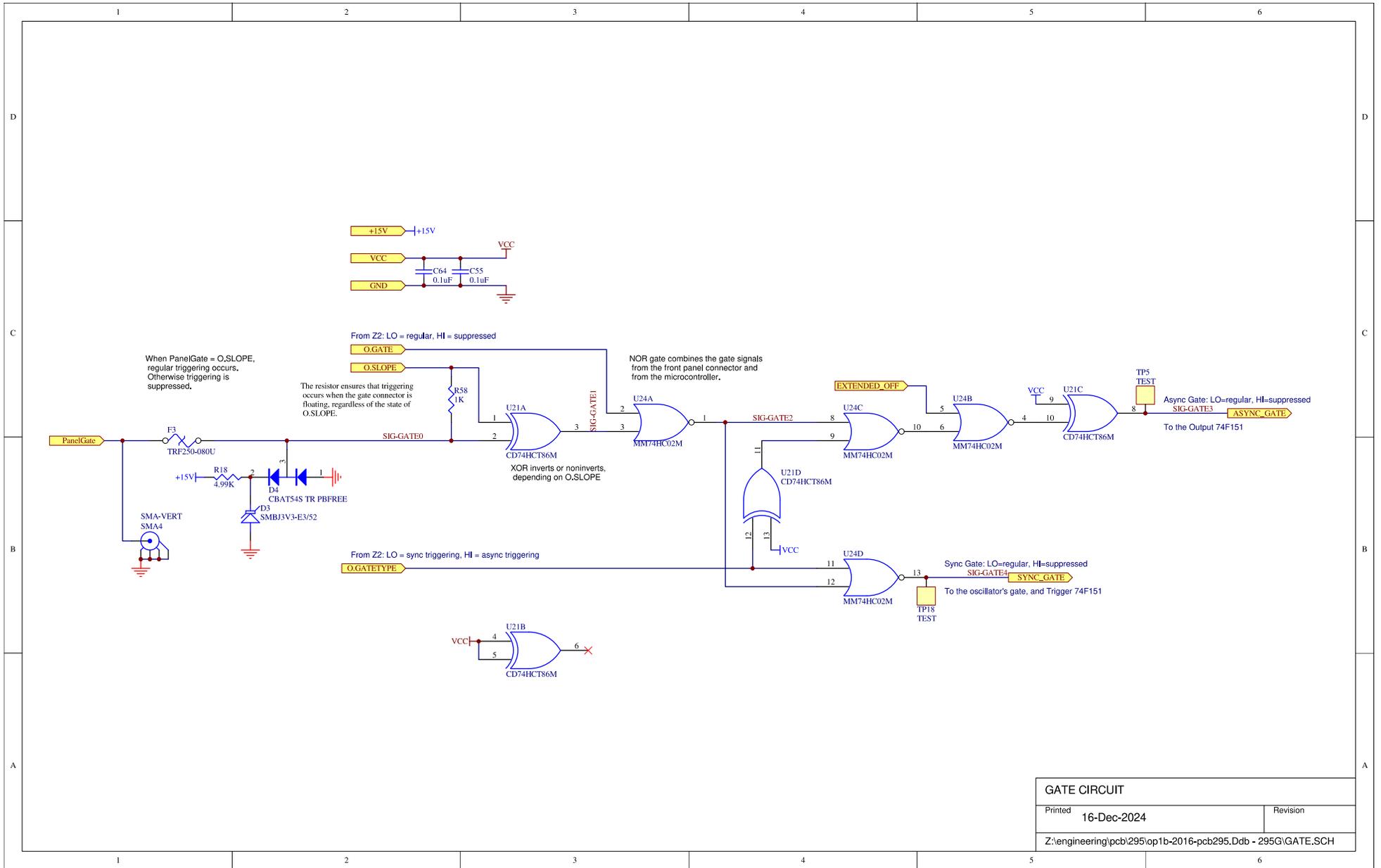


# PCB 295G - MAIN CONTROL BOARD, 6 OF 13, TIMING TOP-LEVEL

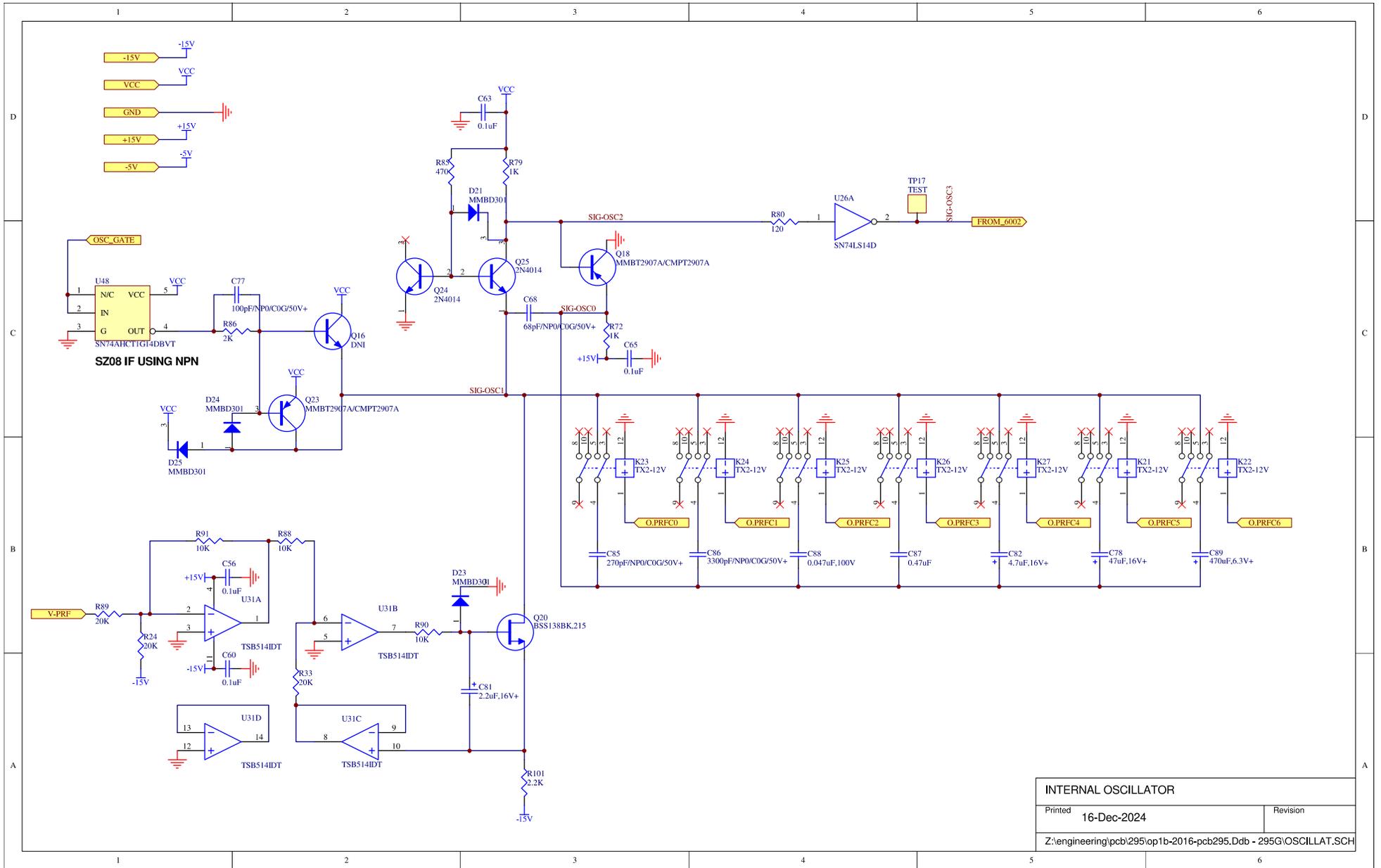


TIMING TOP-LEVEL SCHEMATIC	
Printed	Revision
16-Dec-2024	
Z:\engineering\pcb\295\op1b-2016-pcb295.Ddb - 295G\OP1B-PG_P RJ	

# PCB 295G - MAIN CONTROL BOARD, 7 OF 13, GATE CIRCUIT

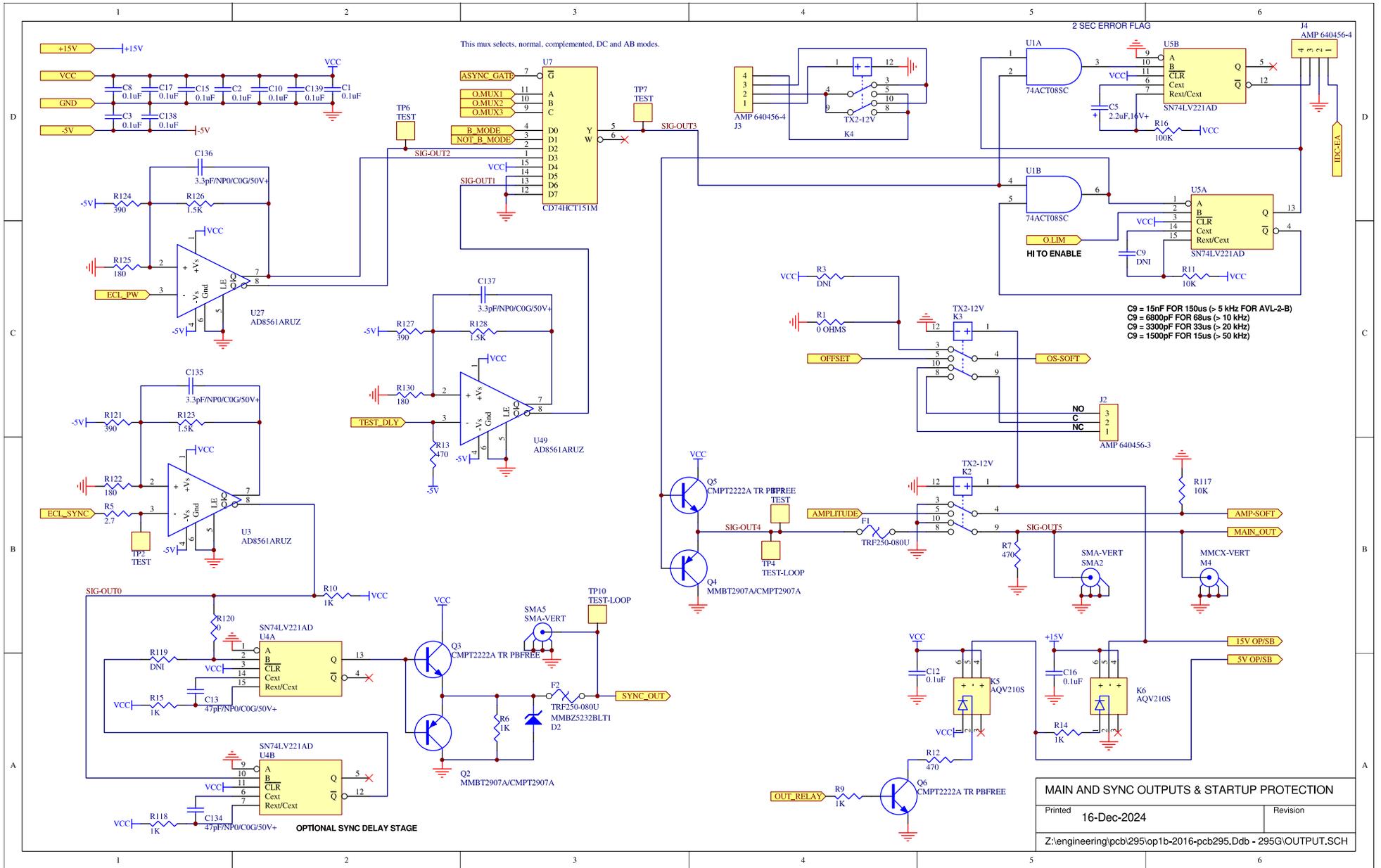


# PCB 295G - MAIN CONTROL BOARD, 8 OF 13, OSCILLATOR



INTERNAL OSCILLATOR	
Printed	Revision
16-Dec-2024	
Z:\engineering\pcb\295\op1b-2016-pcb295.Ddb - 295G\OSCILLAT.SCH	

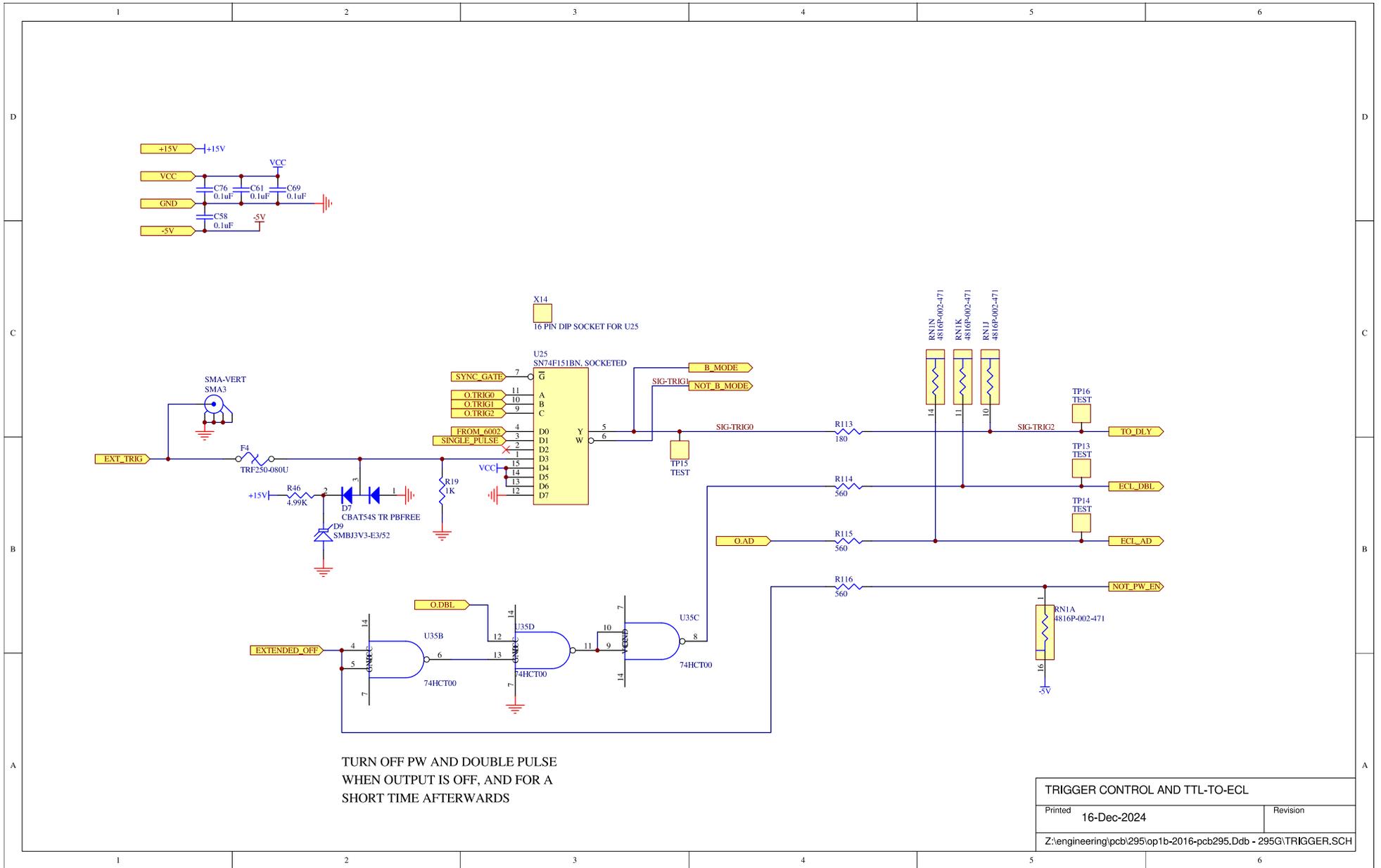
# PCB 295G - MAIN CONTROL BOARD, 9 OF 13, TTL OUTPUTS



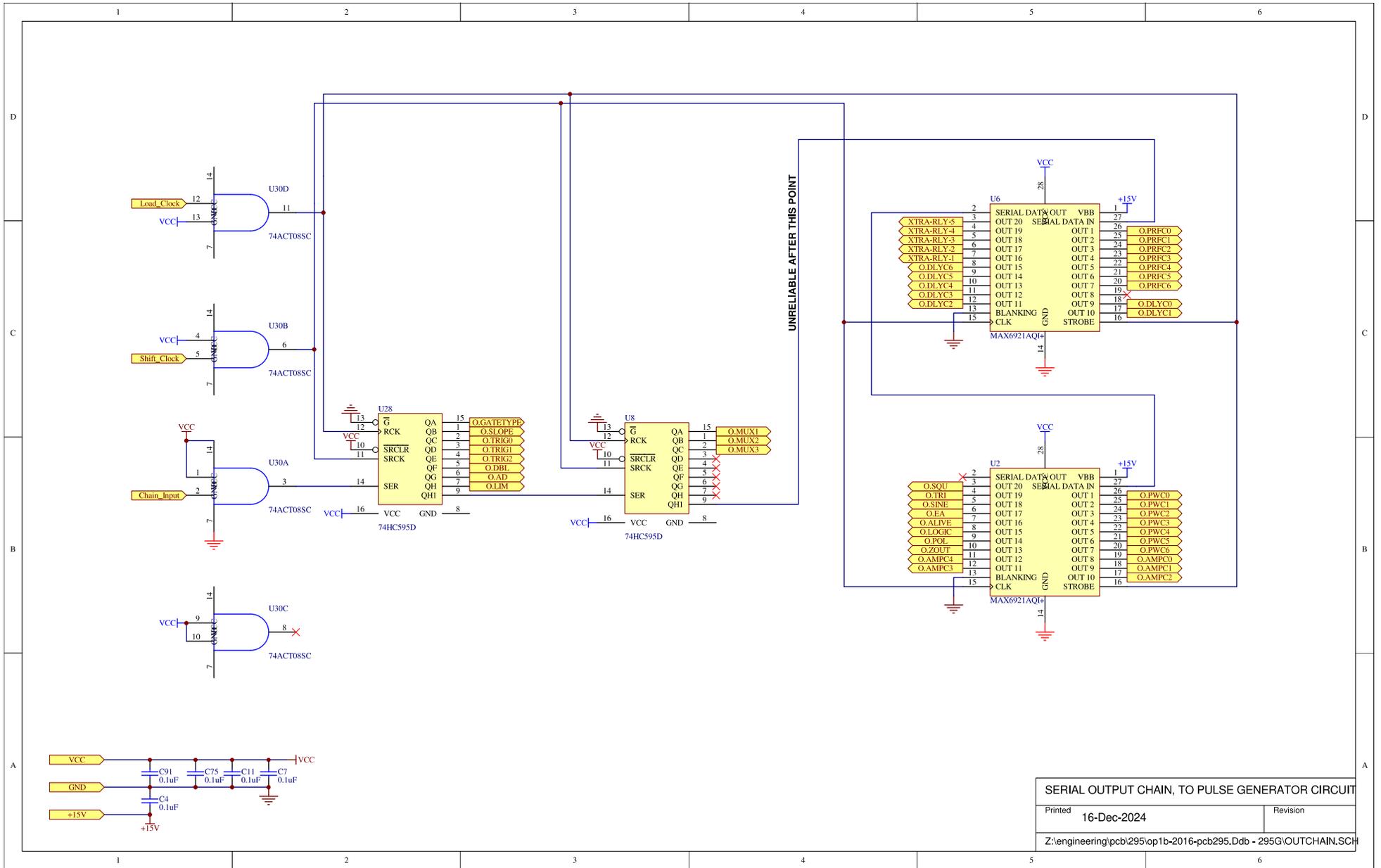




# PCB 295G - MAIN CONTROL BOARD, 12 OF 13, TRIGGER SELECT



# PCB 295G - MAIN CONTROL BOARD, 13 OF 13, SHIFT REGISTERS



SERIAL OUTPUT CHAIN, TO PULSE GENERATOR CIRCUIT	
Printed	16-Dec-2024
Revision	
Z:\engineering\pcb\295\op1b-2016-pcb295.Ddb - 295G\OUTCHAIN.SCH	



PERFORMANCE CHECK SHEET