INSTRUCTIONS

MODEL AVMP-4-EA-EW PULSE GENERATOR

S.N.:

WARRANTY

Avtech Electrosystems Ltd. warrants products of its manufacture to be free from defects in material and workmanship under conditions of normal use. If, within one year after delivery to the original owner, and after prepaid return by the original owner, this Avtech product is found to be defective, Avtech shall at its option repair or replace said defective item. This warranty does not apply to units which have been dissembled, modified or subjected to conditions exceeding the applicable specifications or ratings. This warranty is the extent of the obligation assumed by Avtech with respect to this product and no other warranty or guarantee is either expressed or implied.

TECHNICAL SUPPORT

Phone: 613-226-5772 or 1-800-265-6681
Fax: 613-226-2802 or 1-800-561-1970

E-mail: info@avtechpulse.com
World Wide Web: http://www.avtechpulse.com

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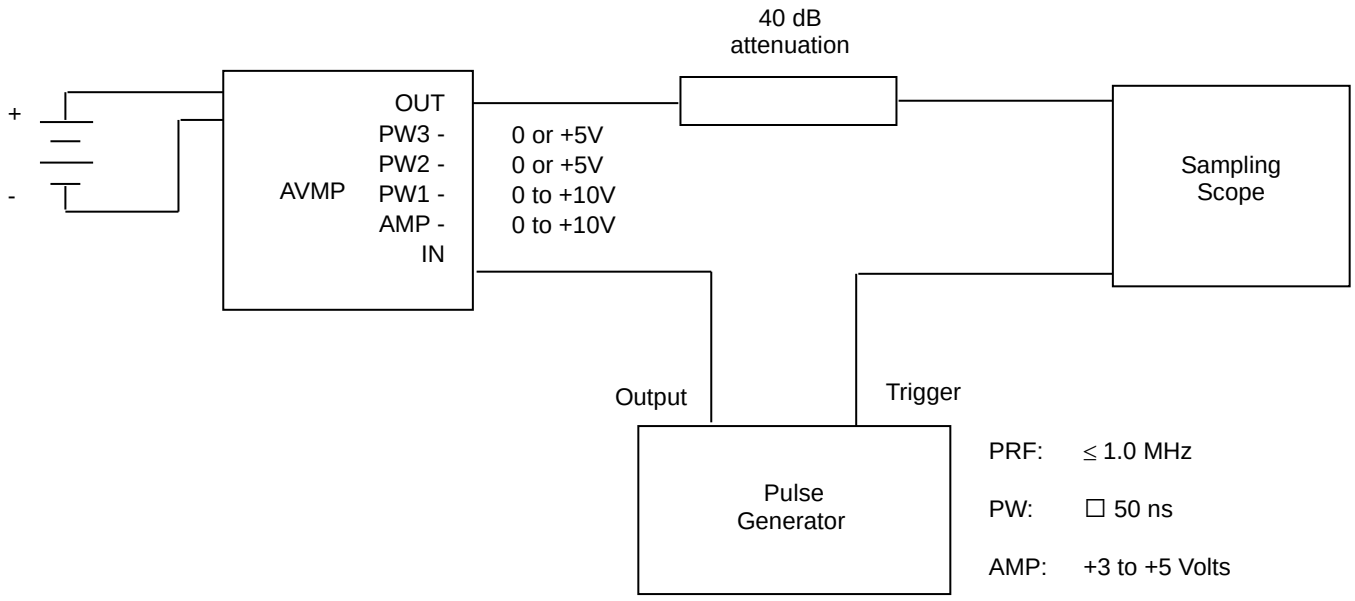
Manual Reference: /fileserver1/officefiles/instructword/avmp/AVMP-4-EA-EW-eda-fig.doc, created January 25, 2001

FIG. 1: AVMP PULSE GENERATOR TEST ARRANGEMENT



GENERAL OPERATING INSTRUCTIONS

1) The bandwidth capability of components and instruments used to display the pulse generator output signal (attenuators, cables, connectors, etc.) should exceed ten gigahertz.

2) The use of 40 db attenuator will insure a peak input signal to the sampling scope of less than one volt.

3) In general, the source pulse generator trigger delay control should be set in the 0.1 to 1.0 us range. Other settings should be as shown in the above diagram.

4) The Model AVMP pulse generator can withstand an infinite VSWR on the output port.

5) WARNING: Model AVMP may fail if triggered at a PRF greater than 1.0 MHz.

6) The PW Out and DC potentials applied to PW1, PW2 & PW3 solder terminals are related as follows:

PW1	PW2	PW3	PW OUT
0 to +10 VDC	OV	OV	10 ns to 100 ns
0 to +10 VDC	+5V VDC	OV	$\leq$ 100 ns to 1 μs
0 to +10 VDC	OV	+ 5 VDC	$\leq$ 1μs to 10 μs

The input resistance to PW1 is $\geq$ 10K while the input resistance to PW 2 and PW 3 is greater than 500 Ohms.

7) The output amplitude is controlled by applying 0 to +10 VDC to the “AMP” solder terminal ($R_{IN} \geq$ 10K).

8) The module should be bolted to a heat sink capable of dissipating at least 10 Watts.

9) For additional assistance:
Tel: (613) 226-5772
Fax: (613) 226-2802
Email: info@avtechpulse.com

FIG. 2: MODEL AVMP-4 CHASSIS (-EA, -EW)

PERFORMANCE CHECK SHEET