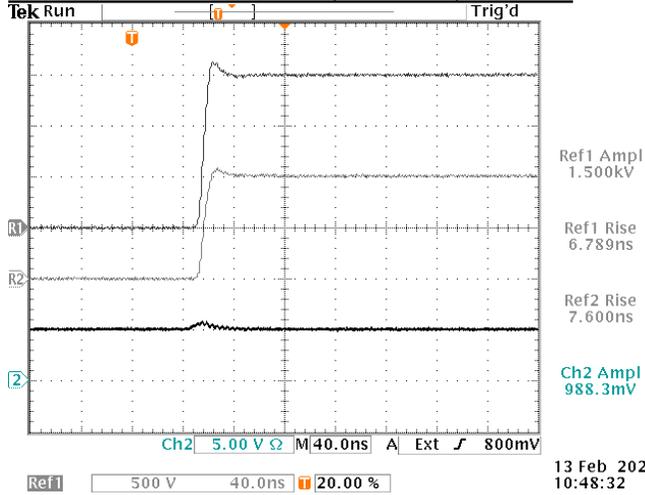


PERFORMANCE CHECKSHEET

Model: AVRQ-5-B-AC22-AHV-ATA3-FPD
 Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers
 S.N.: 14513
 Date: February 13, 2025

Minimum Rise Time Test, No DUT, Positive



a) Output Signal Amplitude: ± 1 to ± 1.5 kV

b) Rise Time (10%-90%): < 10 to > 50 ns

c) PRF: 1 Hz - 10 Hz

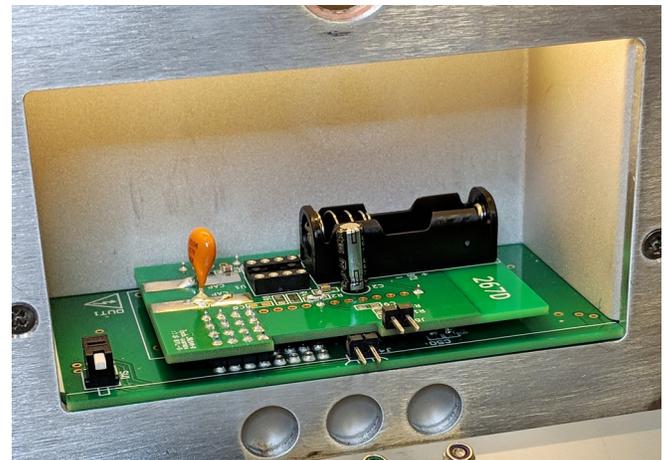
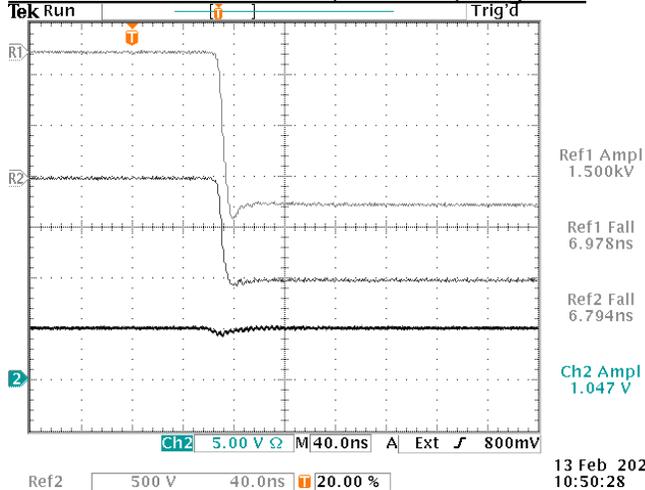
d) Jitter, Stability: OK

e) Prime Power: 100-240V AC, 50-60 Hz.

Top = +1.5 and +1.0 kV HV out (stored - with signal disconnected before recording logic waveform).

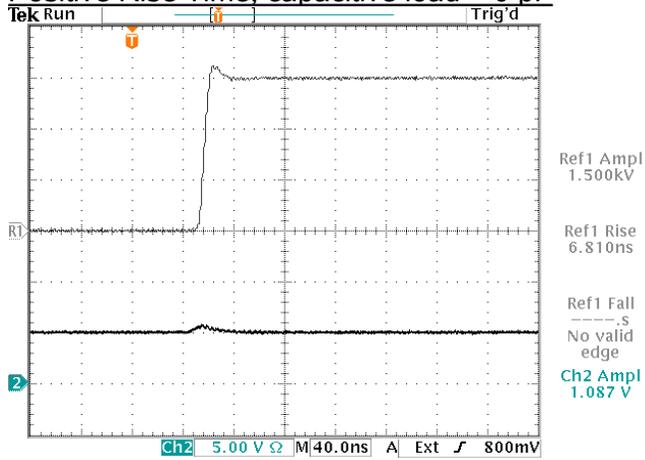
Bottom = Logic "A" out for +1.5 kV, VCC2 = +5V, using P6246, and no DUT, R2 = 1 k Ω . (This shows the parasitic capacitive coupling onto the Logic "A" out.)

Minimum Rise Time Test, No DUT, Negative



Daughterboard installed in positive position (with no DUT IC)

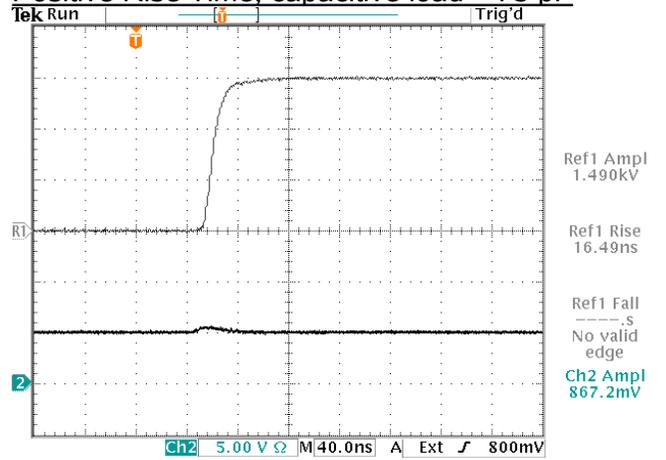
Positive Rise Time, capacitive load = 0 pF



Ref1 500 V 40.0ns 20.00 %

13 Feb 2025 11:03:12

Positive Rise Time, capacitive load = 75 pF

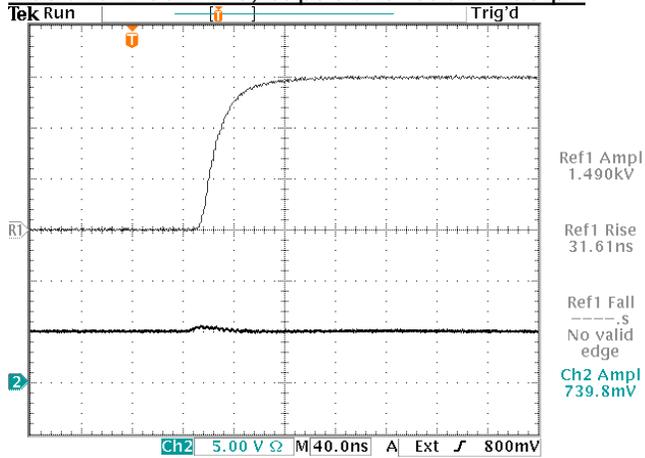


Ref1 500 V 40.0ns 20.00 %

13 Feb 2025 11:02:24

Top = HV out (stored - with signal disconnected before recording logic waveform)
 Bottom = Logic "A" out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

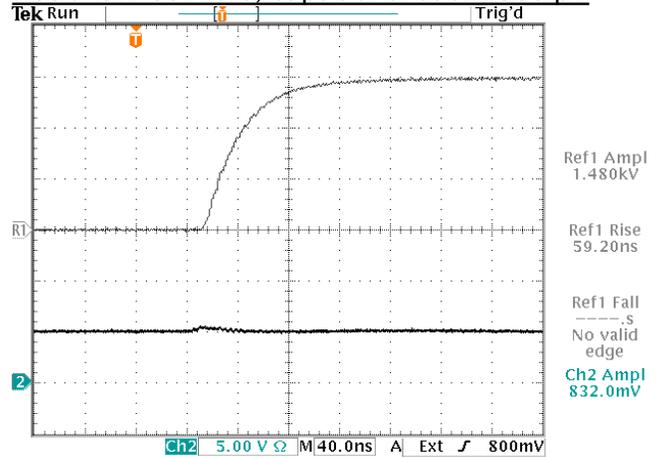
Positive Rise Time, capacitive load = 150 pF



Ref1 500 V 40.0ns 20.00 %

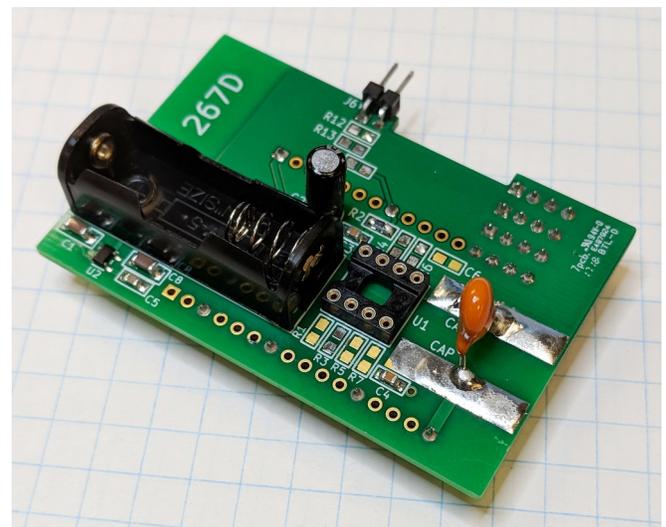
13 Feb 2025 11:00:19

Positive Rise Time, capacitive load = 300 pF



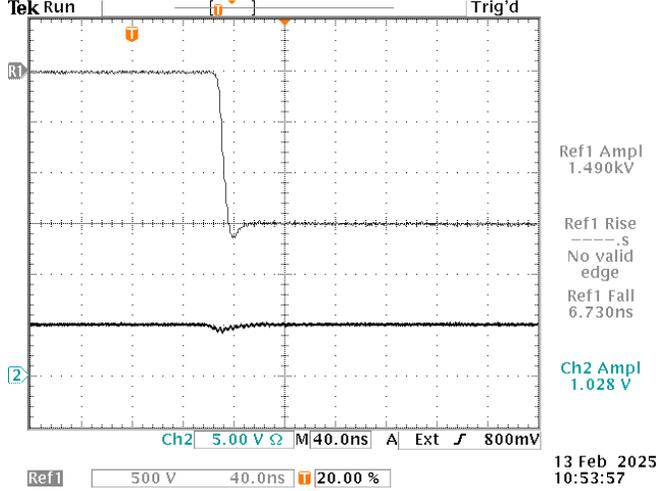
Ref1 500 V 40.0ns 20.00 %

13 Feb 2025 10:59:23

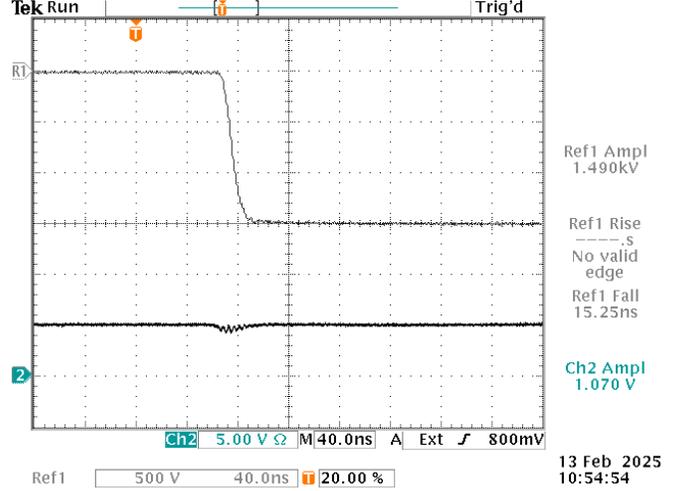


150 pF capacitor (orange) on daughterboard

Negative Rise Time, capacitive load = 0 pF

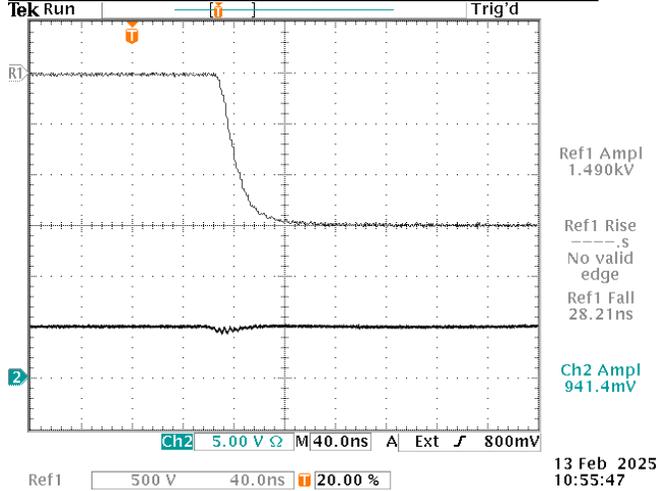


Negative Rise Time, capacitive load = 75 pF

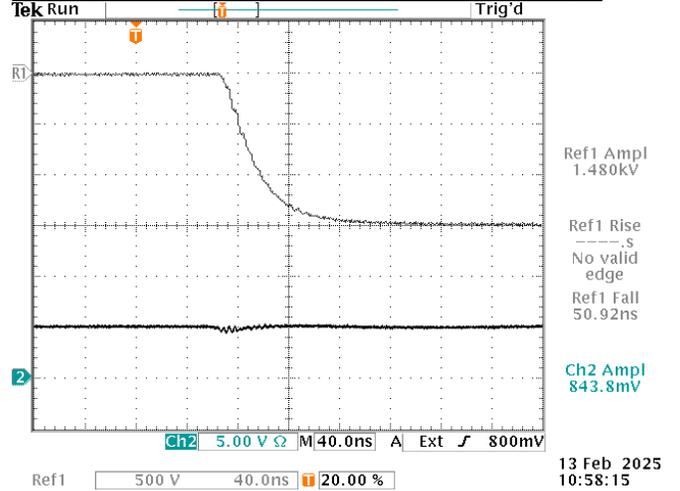


Top = HV out (stored - with signal disconnected before recording logic waveform)
 Bottom = Logic "A" out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

Negative Rise Time, capacitive load = 150 pF

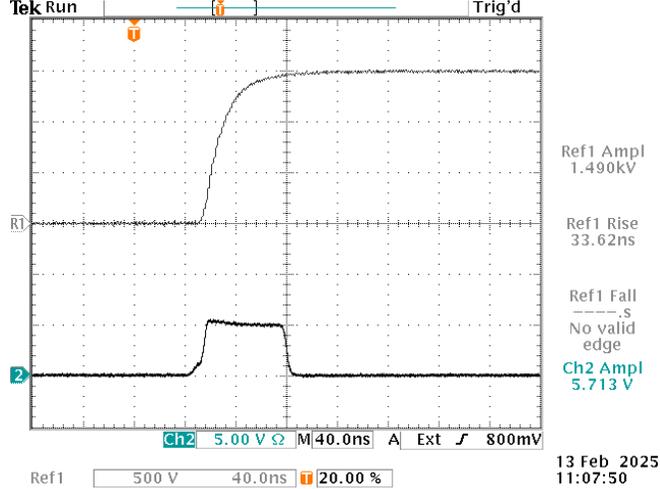


Negative Rise Time, capacitive load = 300 pF

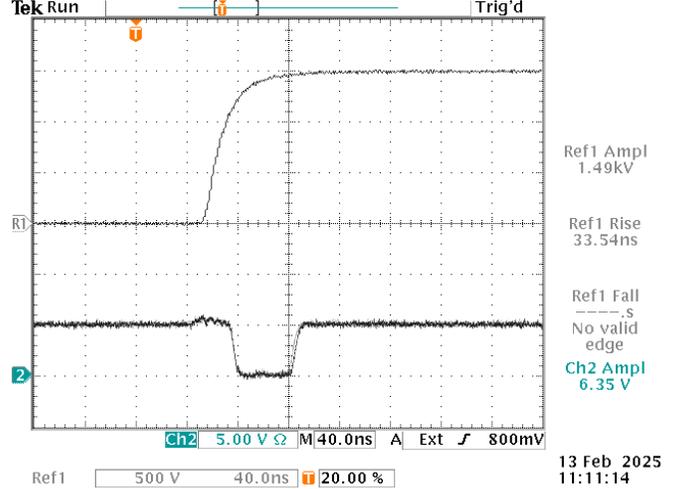


Daughterboard installed in negative position (with no DUT IC)

HCPL-7721, 0V input, +1.5 kV, 150 pF added



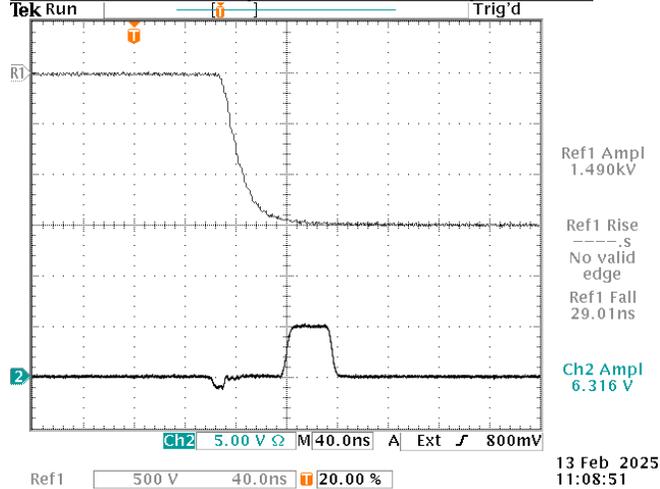
HCPL-7721, 5V input, +1.5 kV, 150 pF added



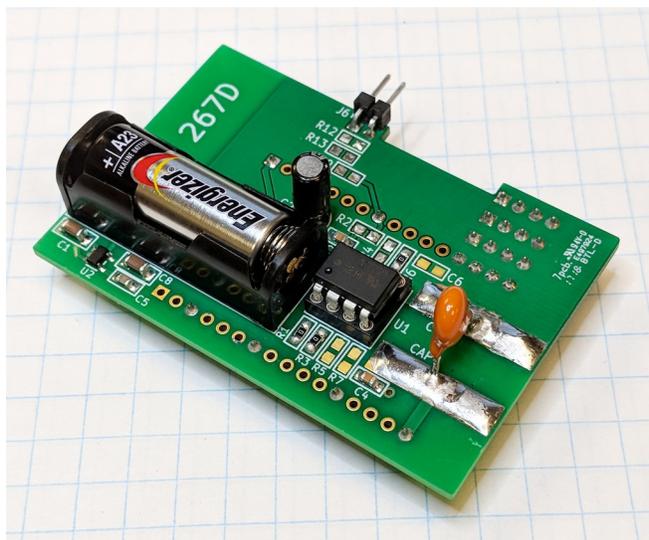
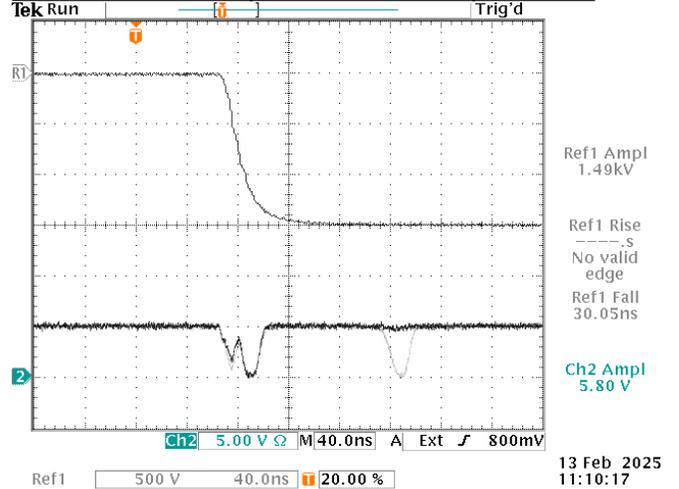
Top = high voltage pulse (stored - with signal disconnected before recording logic waveform).

Bot = Logic "A" out (with 0V input) using P6246.

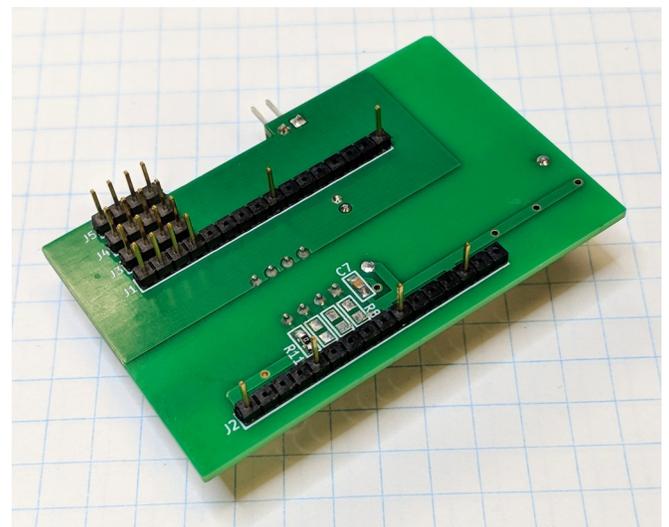
HCPL-7721, 0V input, -1.5 kV, 150 pF added



HCPL-7721, 5V input, -1.5 kV, 150 pF added



Top side of daughterboard with HCPL-7721 configured for 5V bias.



Bottom side of daughterboard with HCPL-7721 configured for 5V bias.