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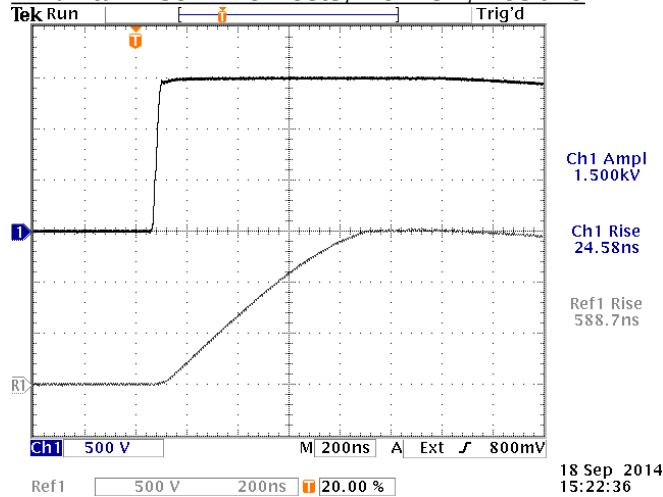
BOX 5120, LCD MERIVALE  
OTTAWA, ONTARIO  
CANADA K2C 3H5

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PERFORMANCE CHECKSHEET

Model: AVRQ-4-B-SCHB-AC03-SO8  
Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers  
S.N.: 13202  
Date: September 19, 2014

Min/Max Rise Time Tests, No DUT, Positive



a) Output Signal Amplitude:  $\pm 1$  kV,  $\pm 1.5$  kV

b) Rise Time (10%-90%): 25 ns - 250 ns

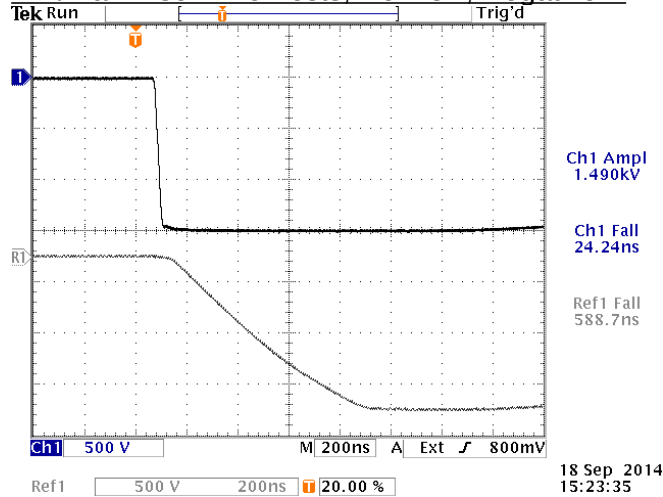
c) PRF: 1 Hz - 10 Hz

d) Jitter, Stability: OK

e) Prime Power: 100-240V AC, 50-60 Hz.

Top: minimum rise time setting, +1.5 kV  
Bottom: maximum rise time setting, +1.5 kV

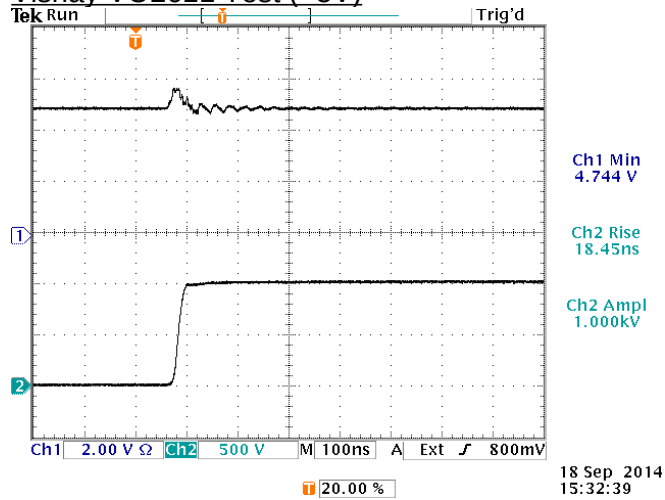
Min/Max Rise Time Tests, No DUT, Negative V



Top: minimum rise time setting, -1.5 kV  
Bottom: maximum rise time setting, -1.5 kV

References levels: 10%, 90%.

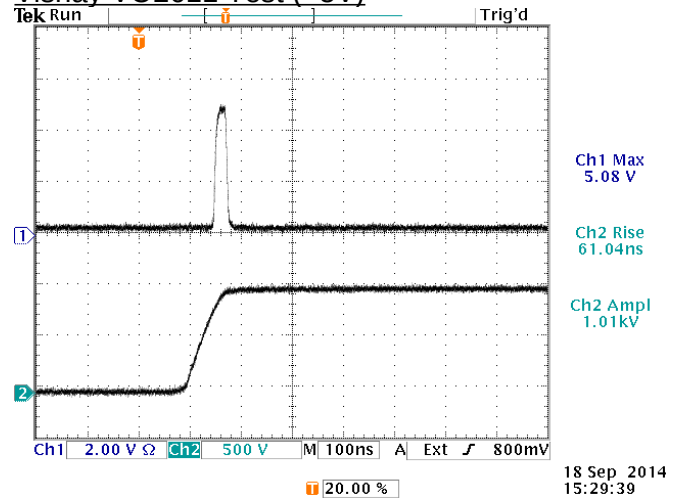
### Vishay VO2611 Test (+5V)



+1 kV, +5V, 0 mA, 348Ω load ("A" PCB).

No glitches at minimum risetime, so the CMTI exceeds  $(1\text{kV} \times (90\% - 10\%) / 18.45 \text{ ns}) = 43.4 \text{ kV/us}$ .

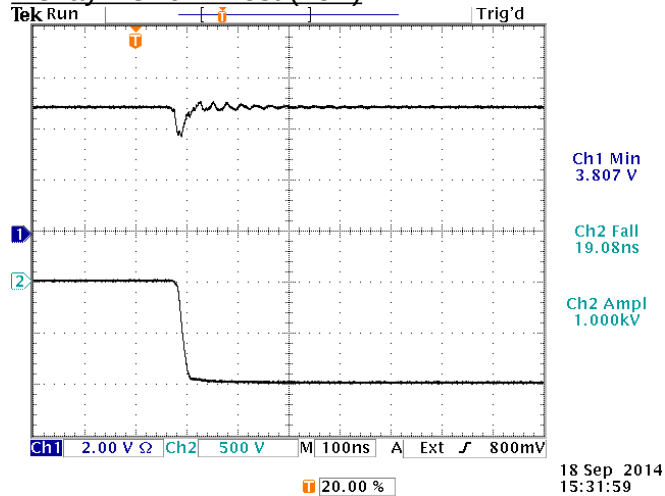
### Vishay VO2611 Test (+5V)



+1 kV, +5V, 7.5 mA, 348Ω load ("D7" PCB).

A ~50% glitch starts to occur at  $1 \text{ kV} \times (90\% - 10\%) / 61.04 \text{ ns} = 13.1 \text{ kV/us}$ .

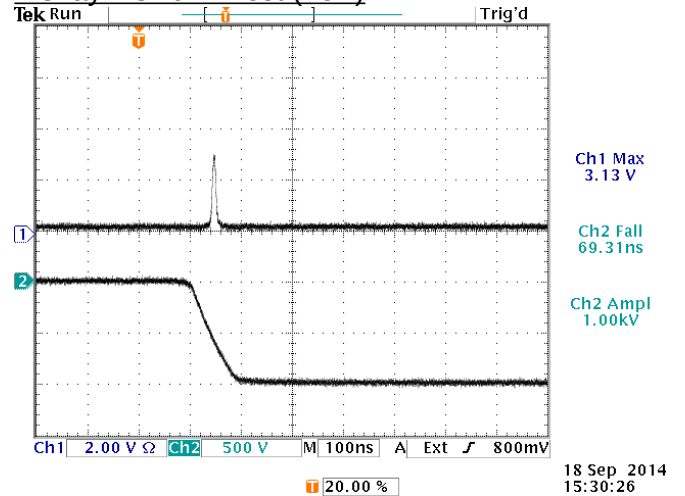
### Vishay VO2611 Test (+5V)



-1 kV, +5V, 0 mA, 348Ω load ("A" PCB).

The glitch at minimum risetime does not dip below 50%, so the CMTI exceeds  $(1\text{kV} \times (90\% - 10\%) / 19.08 \text{ ns}) = 41.9 \text{ kV/us}$ .

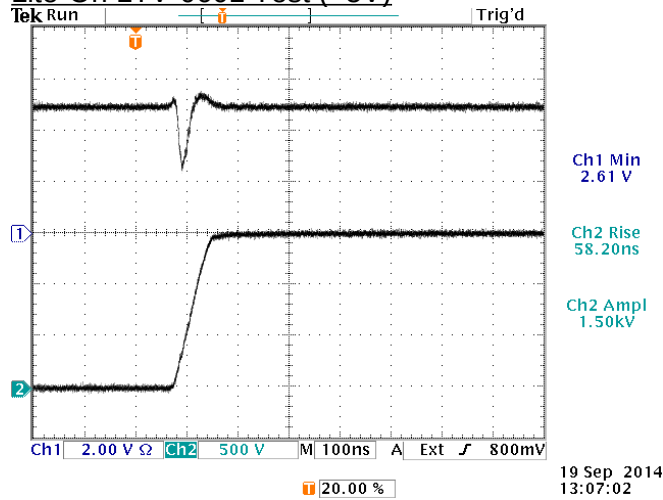
### Vishay VO2611 Test (+5V)



-1 kV, +5V, 7.5 mA, 348Ω load ("D7" PCB).

A ~50% glitch starts to occur at  $1 \text{ kV} \times (90\% - 10\%) / 69.31 \text{ ns} = 11.5 \text{ kV/us}$ .

### Lite-On LTV-0601 Test (+5V)

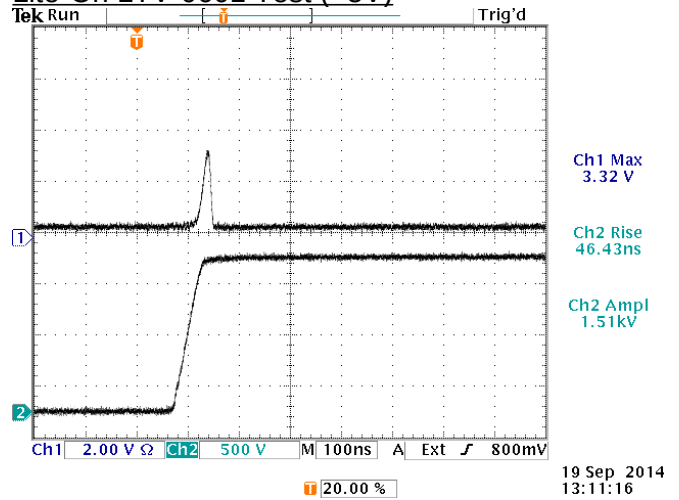


+1.5 kV, +5V, 0 mA, 348Ω load.

R6,8,9,10,11 = 0Ω, R2 = 348Ω, C6 = 15pF, using PCB 263A (SO8 daughterboard)

A ~50% glitch starts to occur at  $1.5 \text{ kV} \times (90\% - 10\%) / 58.2 \text{ ns} = 20.6 \text{ kV/us}$ .

### Lite-On LTV-0601 Test (+5V)

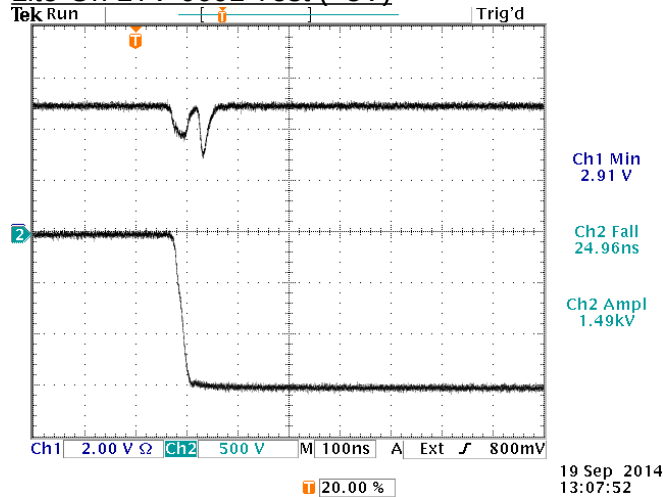


+1.5 kV, +5V, 7.5 mA, 348Ω load.

R6,8,10,11 = 0Ω, R3 = 470Ω, R2 = 348Ω, C6 = 15pF, using PCB 263A (SO8 daughterboard)

A ~50% glitch starts to occur at  $1.5 \text{ kV} \times (90\% - 10\%) / 46.43 \text{ ns} = 25.8 \text{ kV/us}$ .

### Lite-On LTV-0601 Test (+5V)

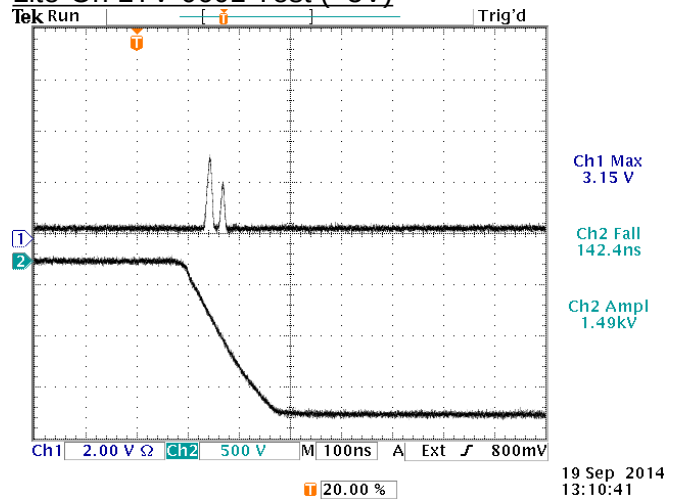


-1.5 kV, +5V, 0 mA, 348Ω load.

R6,8,9,10,11 = 0Ω, R2 = 348Ω, C6 = 15pF, using PCB 263A (SO8 daughterboard)

The glitch at minimum risetime does not dip below 50%, so the CMTI exceeds  $(1.5 \text{ kV} \times (90\% - 10\%) / 24.96 \text{ ns}) = 48.1 \text{ kV/us}$ .

### Lite-On LTV-0601 Test (+5V)



-1.5 kV, +5V, 7.5 mA, 348Ω load.

R6,8,10,11 = 0Ω, R3 = 470Ω, R2 = 348Ω, C6 = 15pF, using PCB 263A (SO8 daughterboard)

A ~50% glitch starts to occur at  $1.5 \text{ kV} \times (90\% - 10\%) / 142.4 \text{ ns} = 8.4 \text{ kV/us}$ .