PERFORMANCE CHECKSHEET

Model: AVRQ-5-B-AC22-AHV-CC1-ID1-VXI-HF-V2-X2
Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers
S.N.: 13920
Date: October 9, 2019

Minimum Rise Time Test, No DUT, Positive

- Output Signal Amplitude: ±1 to ±1.5 kV
- Rise Time (10%-90%): < 10 to > 50 ns
- PRF: 1 Hz - 10 Hz
- Jitter, Stability: OK
- Prime Power: 100-240V AC, 50-60 Hz.

Top = +1.5 and +1.0 kV HV out (stored - with signal disconnected before recording logic waveform).

Bottom = Logic “A” out for +1.5 kV, VCC2 = +5V, using P6246, and no DUT, R2 = 1 kΩ. (This shows the parasitic capacitive coupling onto the Logic “A” out.)

Minimum Rise Time Test, No DUT, Negative

Daughterboard installed in positive position (with no DUT IC)
Positive Rise Time, capacitive load = 0 pF

Top = HV out (stored - with signal disconnected before recording logic waveform)
Bottom = Logic “A” out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

Positive Rise Time, capacitive load = 75 pF

Positive Rise Time, capacitive load = 150 pF

Positive Rise Time, capacitive load = 300 pF

Positive Rise Time, capacitive load = 600 pF

150 pF capacitor (orange) on daughterboard
Negative Rise Time, capacitive load = 0 pF

Top = HV out (stored - with signal disconnected before recording logic waveform)
Bottom = Logic “A” out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

Negative Rise Time, capacitive load = 75 pF

Daughterboard installed in negative position (with no DUT IC)

Negative Rise Time, capacitive load = 150 pF

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Effective Rise Time

Negative Rise Time, capacitive load = 600 pF
VO3120 Test, Fast, 0 mA input, +1.5 kV pulse

Top = HV out (stored - with signal disconnected before recording logic waveform

VO3120 Test, Fast, 10 mA input, +1.5 kV pulse

Top side of daughterboard with VO3120 configured for 10 mA bias.

VO3120 Test, Fast, 0 mA input, -1.5 kV pulse

VO3120 Test, Fast, 10 mA input, -1.5 kV pulse

Bottom side of daughterboard with VO3120 configured for 10 mA bias.

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Top = HV out (stored - with signal disconnected before recording logic waveform

For these tests, 300 pF of capacitance was used.
HCPL-7721, 0V input, +1.5 kV, 150 pF added

Top = high voltage pulse (stored - with signal disconnected before recording logic waveform).
Bot = Logic “A” out (with 0V input) using P6246.

HCPL-7721, 5V input, +1.5 kV, 150 pF added

Top side of daughterboard with HCPL-7721 configured for 5V bias.

HCPL-7721, 5V input, -1.5 kV, 150 pF added

Bottom side of daughterboard with HCPL-7721 configured for 5V bias.

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