PERFORMANCE CHECKSHEET

Model: AVRQ-5-B-AHV-FPD-AC02-ATA3
Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers
S.N.: 13560 (upgrade)
Date: August 16, 2018

Minimum Rise Time Test, No DUT, Positive

- Top = +1.5 and +1.0 kV HV out (stored - with signal disconnected before recording logic waveform).
- Bottom = Logic "A" out for +1.5 kV, VCC2 = +5V, using P6246, and no DUT, R2 = 1 kΩ. (This shows the parasitic capacitive coupling onto the Logic "A" out.)

a) Output Signal Amplitude: ±1 to ±1.5 kV
b) Rise Time (10%-90%): < 10 to > 50 ns
c) PRF: 1 Hz - 10 Hz
d) Jitter, Stability: OK
e) Prime Power: 100-240V AC, 50-60 Hz.

Minimum Rise Time Test, No DUT, Negative

Daughterboard installed in positive position (with no DUT IC)
Positive Rise Time, capacitive load = 0 pF
Top = HV out (stored - with signal disconnected before recording logic waveform)
Bottom = Logic “A” out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

Positive Rise Time, capacitive load = 75 pF

Positive Rise Time, capacitive load = 150 pF

Positive Rise Time, capacitive load = 300 pF

Positive Rise Time, capacitive load = 600 pF

150 pF capacitor (orange) on daughterboard
Negative Rise Time, capacitive load = 0 pF
Top = HV out (stored - with signal disconnected before recording logic waveform)
Bottom = Logic “A” out, VCC2 = +5V, using P6246 probe, and no DUT, R2 = 1 kΩ

Negative Rise Time, capacitive load = 75 pF

Negative Rise Time, capacitive load = 150 pF

Negative Rise Time, capacitive load = 300 pF

Daughterboard installed in negative position (with no DUT IC)
Top = Logic “A” out, +32V VCC2. P6139A probe.
Bottom = HV out (stored - with signal disconnected before recording logic waveform

Top side of daughterboard with VO3120 configured for 10 mA bias.

Bottom side of daughterboard with VO3120 configured for 10 mA bias.
Top = Logic “A” out, +32V VCC2. P6139A probe. Bottom = HV out (stored - with signal disconnected before recording logic waveform

For these tests, 300 pF of capacitance was used.
Top = Logic “A” out (with 0V input) using P6246.
Bottom = high voltage pulse (stored - with signal
disconnected before recording logic waveform).

Top side of daughterboard with HCPL-7721
configured for 5V bias.

Bottom side of daughterboard with HCPL-7721
configured for 5V bias.