

## AVTECH ELECTROSYSTEMS LTD.

NANOSECOND WAVEFORM ELECTRONICS SINCE 1975

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BOX 5120, LCD MERIVALE OTTAWA, CANADA K2C3H5

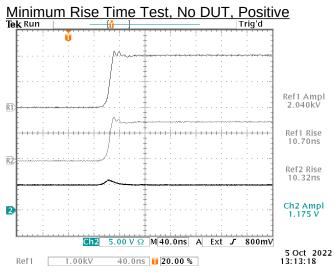
## PERFORMANCE CHECKSHEET

Model: AVRQ-5-B-XHV-AC22

Type: Common Mode Transient Immunity (CMTI) Test for Opto-Couplers

S.N.: 14280

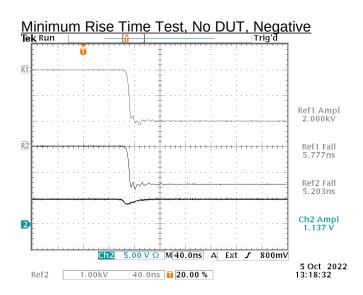
Date: October 5, 2022



Top = +1.5 and +2.0 kV HV out (stored - with signal disconnected before recording logic waveform).

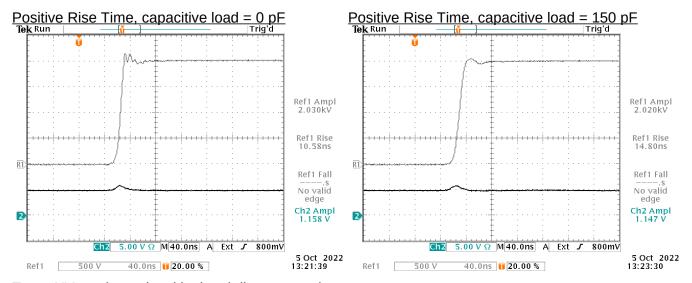
Bottom = Logic "A" out for +U+0032 kV, VCC2 = +5V, using P6246, and no DUT, R2 = 1 k $\Omega$ . (This shows the parasitic capacitive coupling onto the Logic "A" out.)

- a) Output Signal Amplitude: ±1.5 to ±2 kV
- b) Rise Time (10%-90%): < 15 to > 50 ns
- c) PRF: 1 Hz 100 Hz
- d) Jitter, Stability: OK
- e) Prime Power: 100-240V AC, 50-60 Hz.

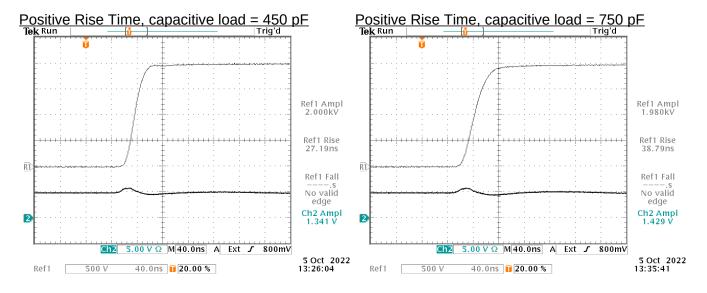


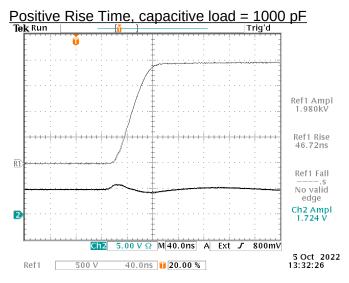


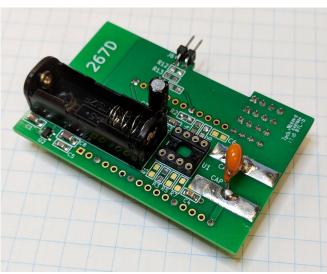
Daughterboard installed in positive position (with no DUT IC)



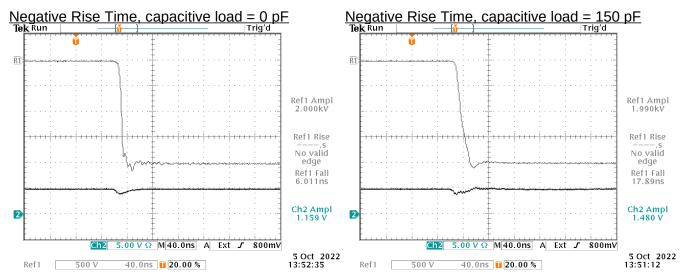
Top = HV out (stored - with signal disconnected before recording logic waveform) Bottom = Logic "A" out, VCC2 = +5V, using P6246 probe, and no DUT, R2 =  $1 \text{ k}\Omega$ 



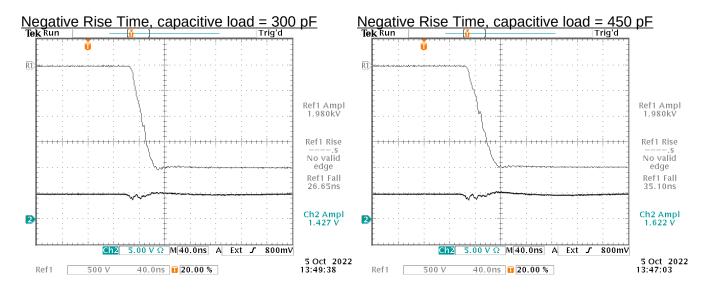


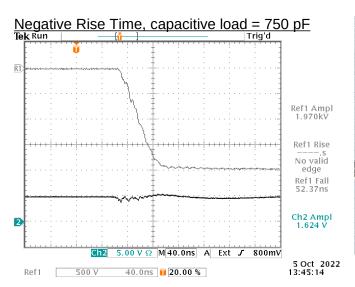


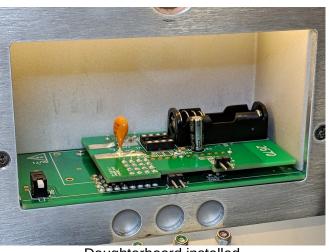
150 pF capacitor (orange) on daughterboard



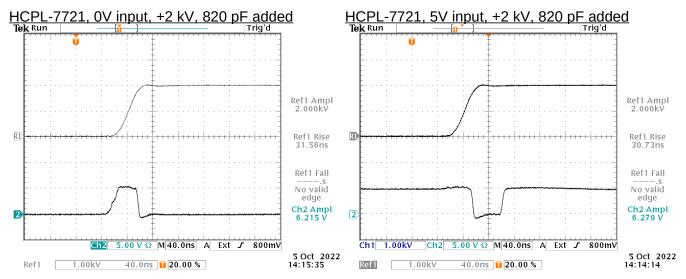
Top = HV out (stored - with signal disconnected before recording logic waveform) Bottom = Logic "A" out, VCC2 = +5V, using P6246 probe, and no DUT, R2 =  $1 \text{ k}\Omega$ 





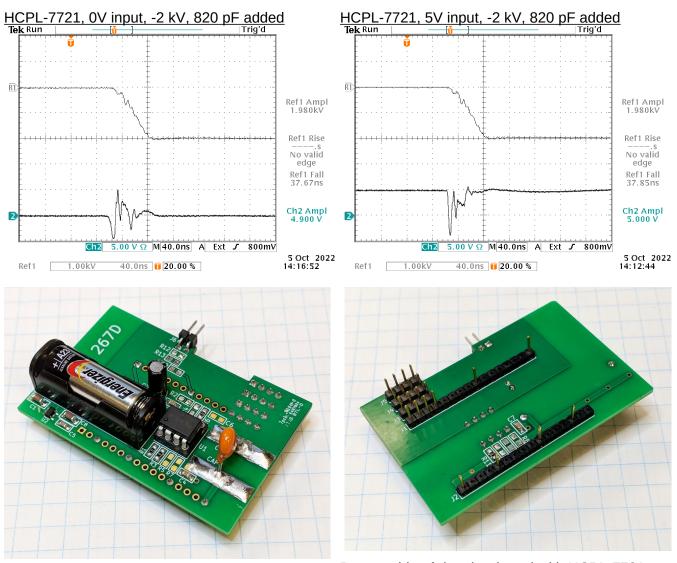


Daughterboard installed in negative position (with no DUT IC)



Top = high voltage pulse (stored - with signal disconnected before recording logic waveform).

Bot = Logic "A" out (with 0V input) using P6246.



Top side of daughterboard with HCPL-7721 configured for 5V bias.

Bottom side of daughterboard with HCPL-7721 configured for 5V bias.